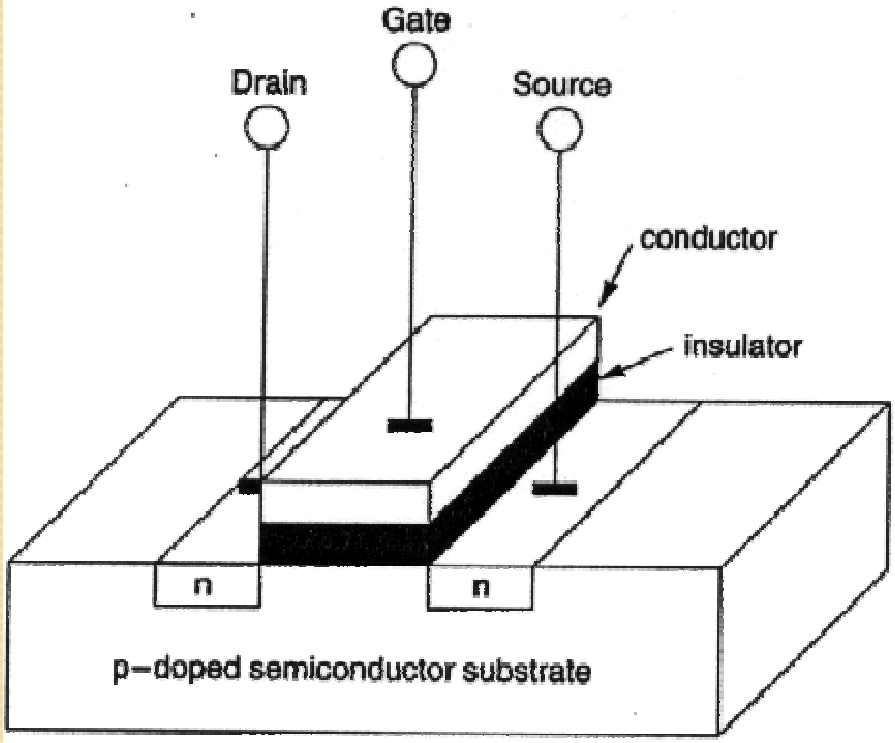
CMOS Technology

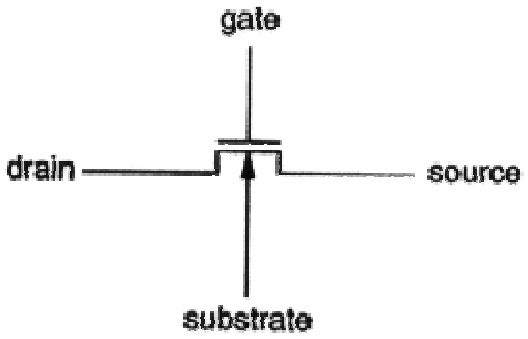
- NMOS
- PMOS
- CMOS
- Logic Gates using CMOS
- Layout

NMOS Structure

- Gate (Metal -> Polysilicon)
- Insulator (Oxide -> Silicon dioxide)
- Substrate (Semiconductor : Si, SiGe)

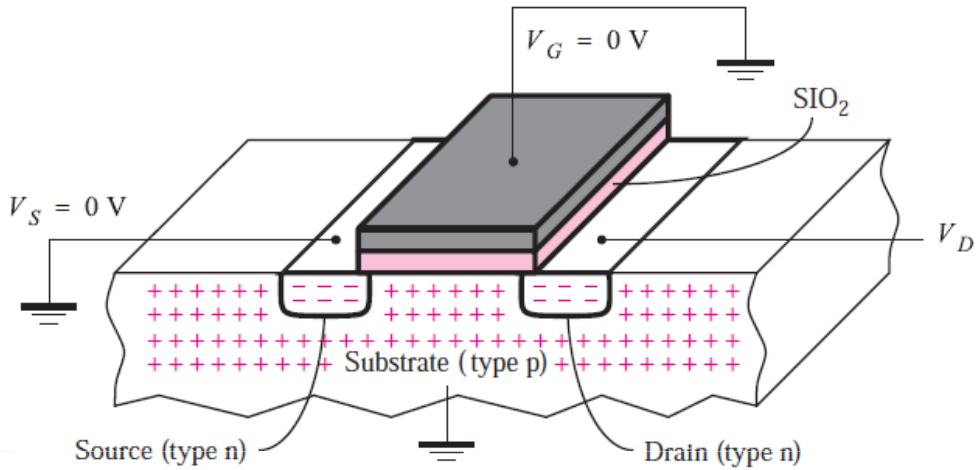


n–transistor

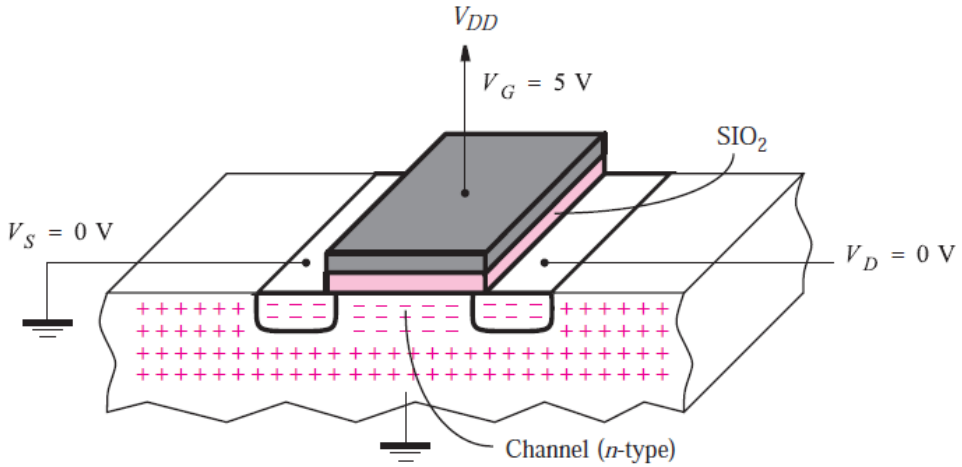


Schematic Icon

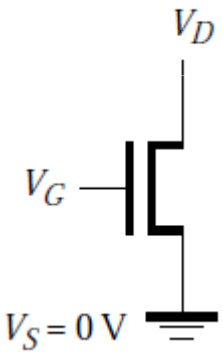
NMOS Operations



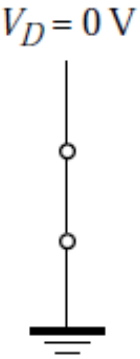
(a) When V_{GS} = 0 V, the transistor is off



(b) When V_{GS} = 5 V, the transistor is on



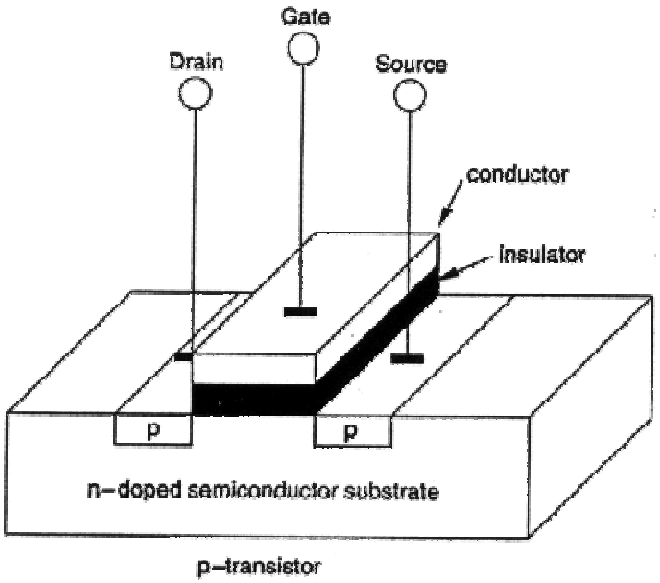
Open switch when $V_G = 0$ V



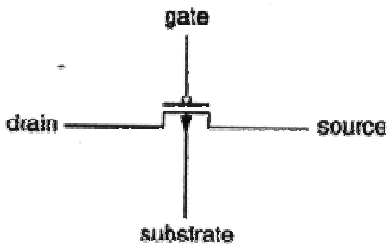
Closed switch when $V_G = V_{DD}$

[Adapted from Fundamentals of Digital Logic by Brown & Vranesic]

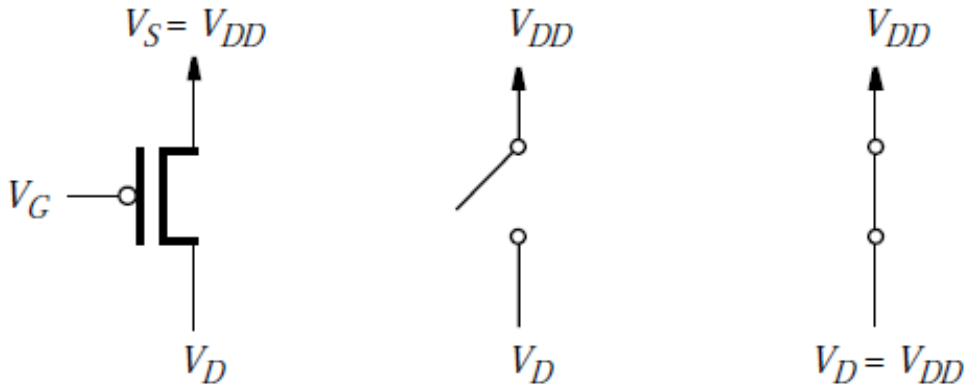
PMOS structure & operations



p–transistor



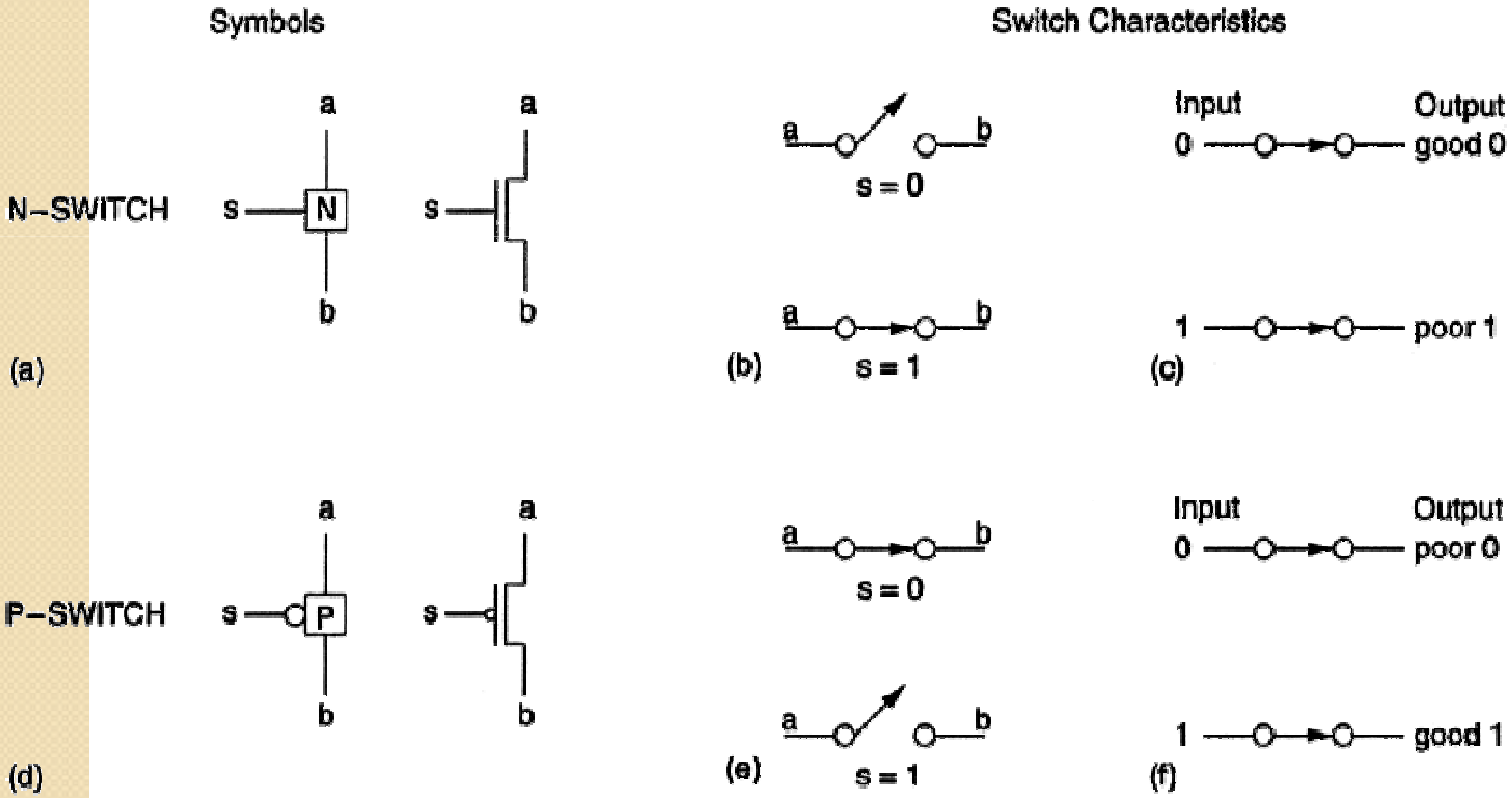
Schematic Icon



Open switch when $V_G = V_{DD}$

Closed switch when $V_G = 0$ V

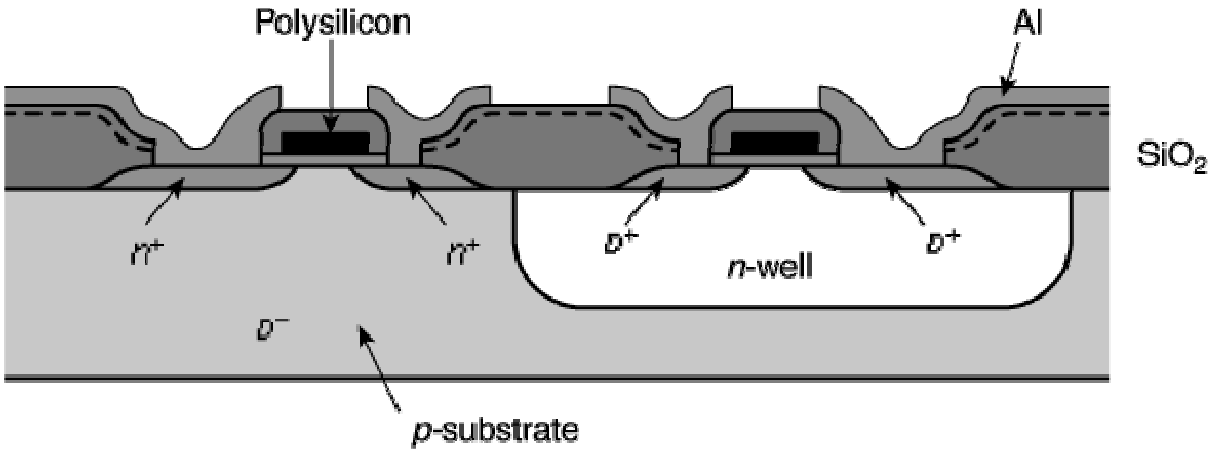
Switch-Level View of NMOS & PMOS

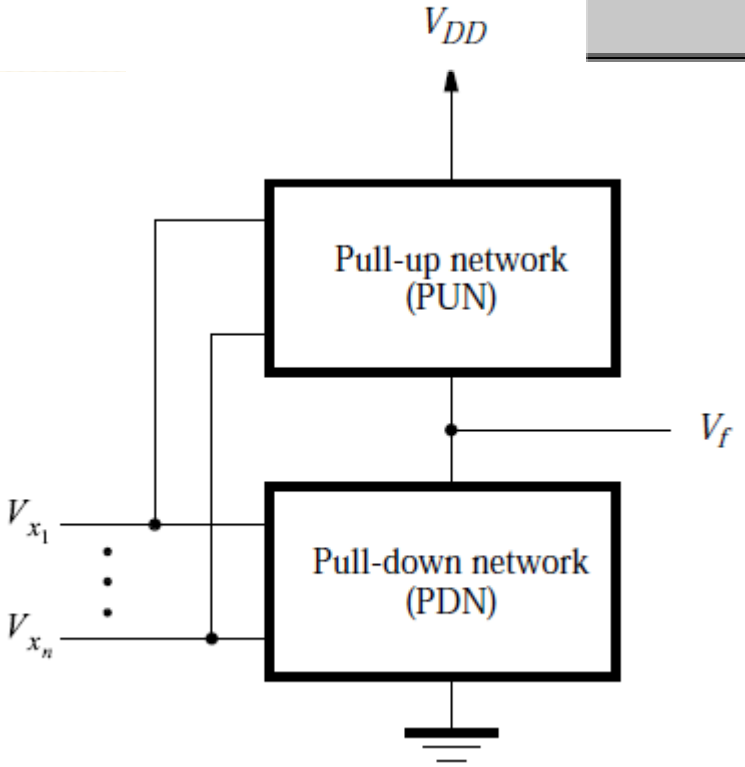


[Adapted from Principles of CMOS VLSI Design by Weste & Eshraghian]

CMOS

- CMOS = Complementary MOS = NMOS + PMOS



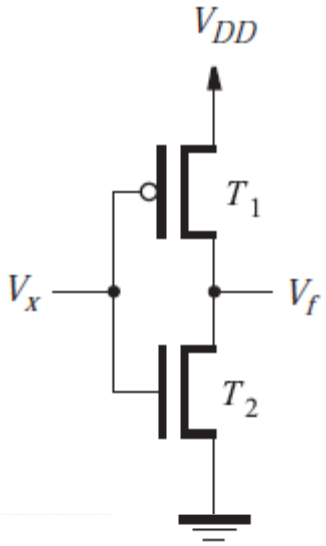


PMOS

NMOS

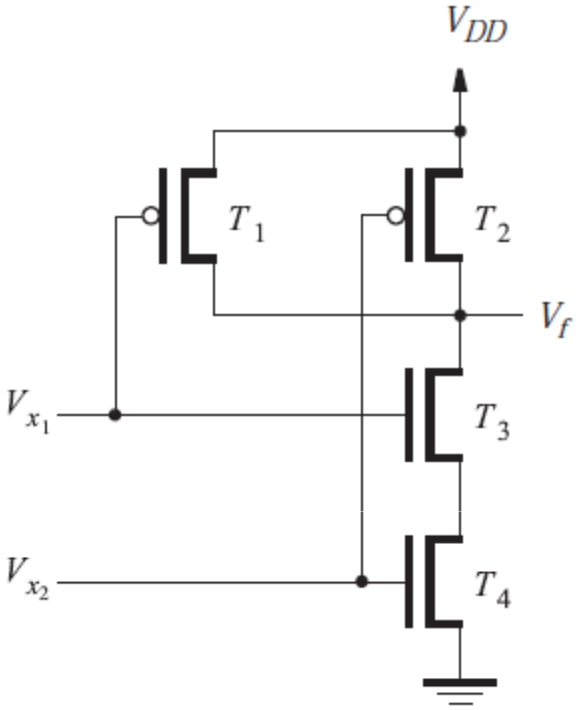
CMOS Logic Gate Structure

CMOS Logic Gates



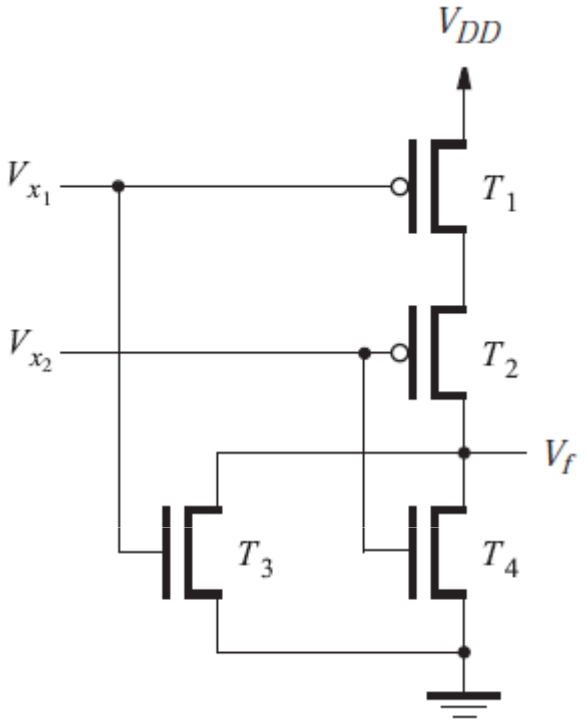
x	T_1	T_2	f
0	on	off	1
1	off	on	0

Inverter



x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	on	on	off	off	1
0	1	on	off	off	on	1
1	0	off	on	on	off	1
1	1	off	off	on	on	0

NAND



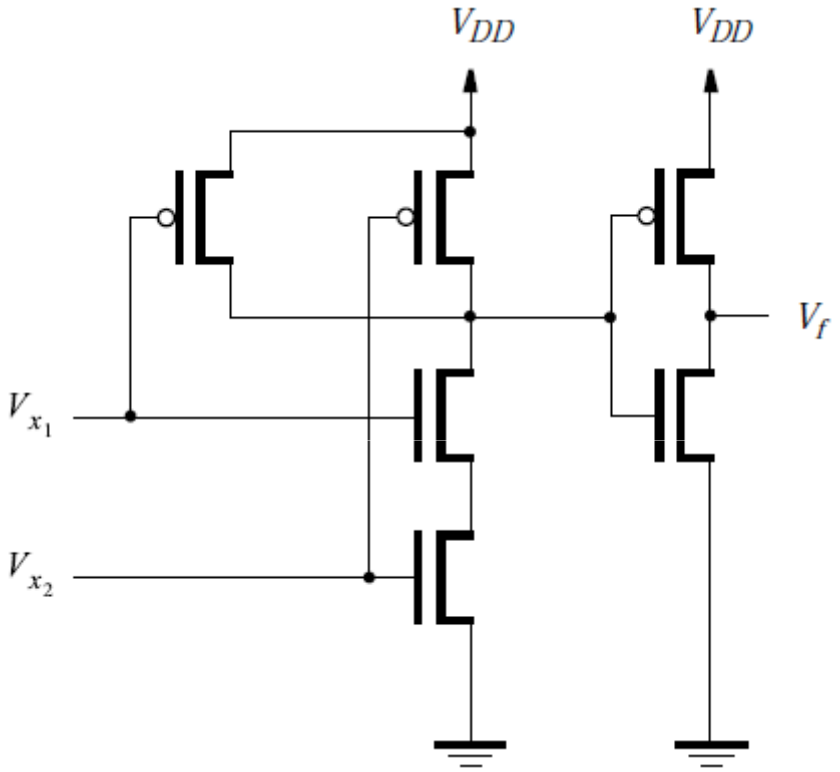
x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	on	on	off	off	1
0	1	on	off	off	on	0
1	0	off	on	on	off	0
1	1	off	off	on	on	0

NOR

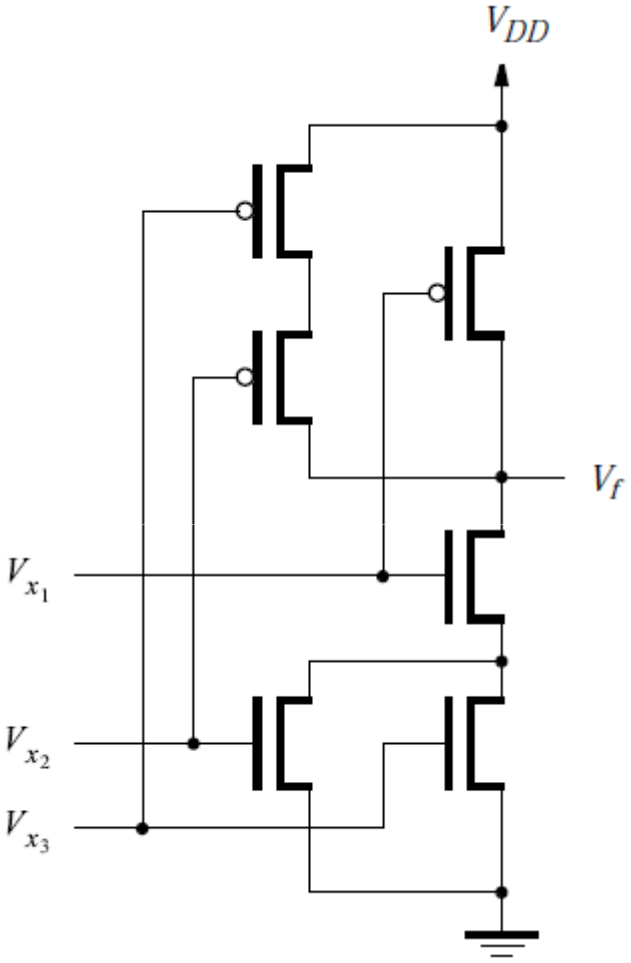
Required Conditions

- NAND:
  - PUN : consider $f = 1$ (i.e., $f = (x_1\ x_2)'$) when $x_1 = 0$ or $x_2 = 0$, thus inputs x_1, x_2 "in parallel"
  - PDN : consider $f = 0$ (i.e., $f' = x_1\ x_2$) when $x_1 = 1$ and $x_2 = 1$, thus x_1, x_2 "in series"
- NOR: the opposite to NAND
  - PUN : consider $f = 1$ (i.e., $f = (x_1 + x_2)'$) when both $x_1 = 0$ and $x_2 = 0$, thus inputs x_1, x_2 "in series"
  - PDN : consider $f = 0$ (i.e., $f' = x_1 + x_2$) when $x_1 = 1$ or $x_2 = 1$, thus x_1, x_2 "in parallel"
- Note that AND -> "series", OR -> "parallel".

CMOS Circuits

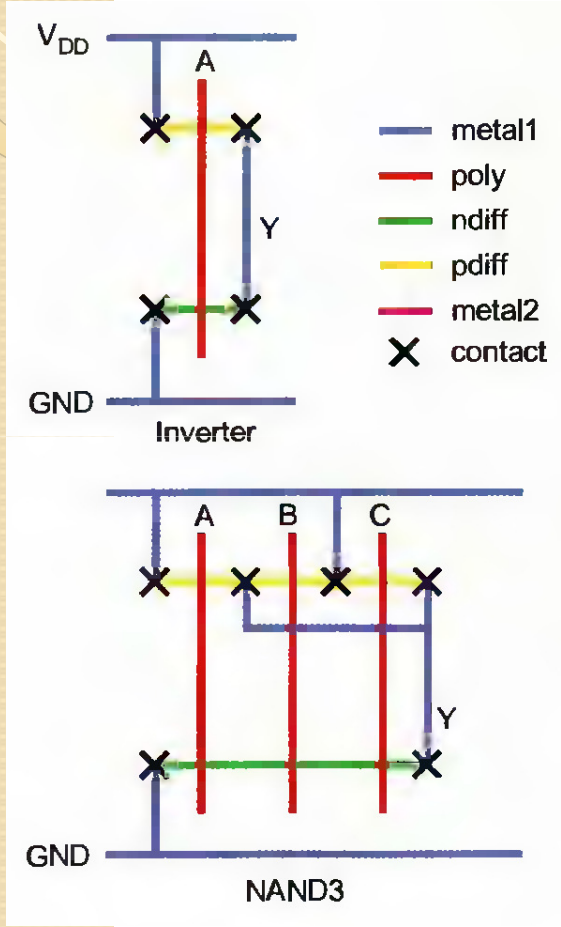


AND

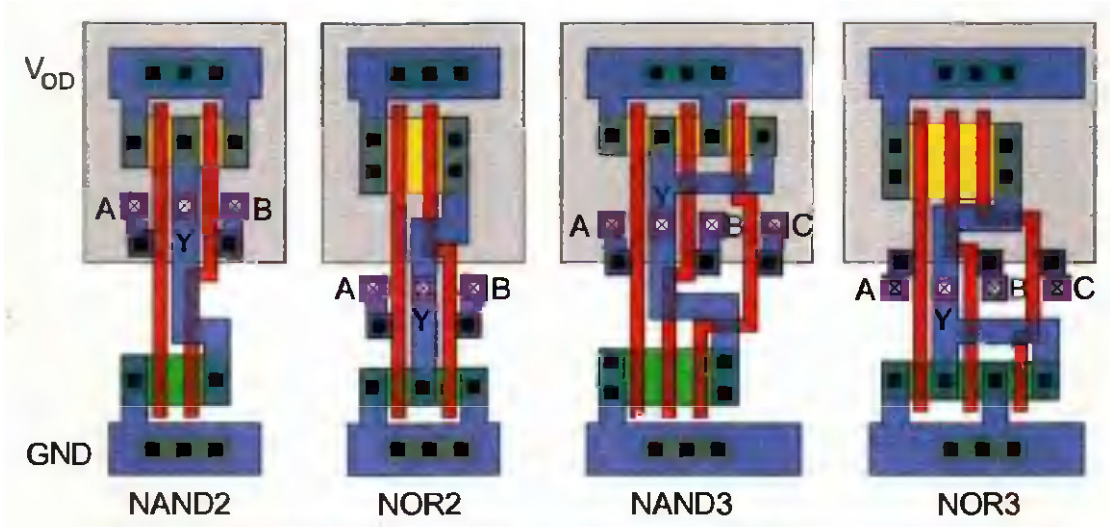


$$f = \bar{x}_1 + \bar{x}_2\bar{x}_3$$

Stick Diagram & Layout

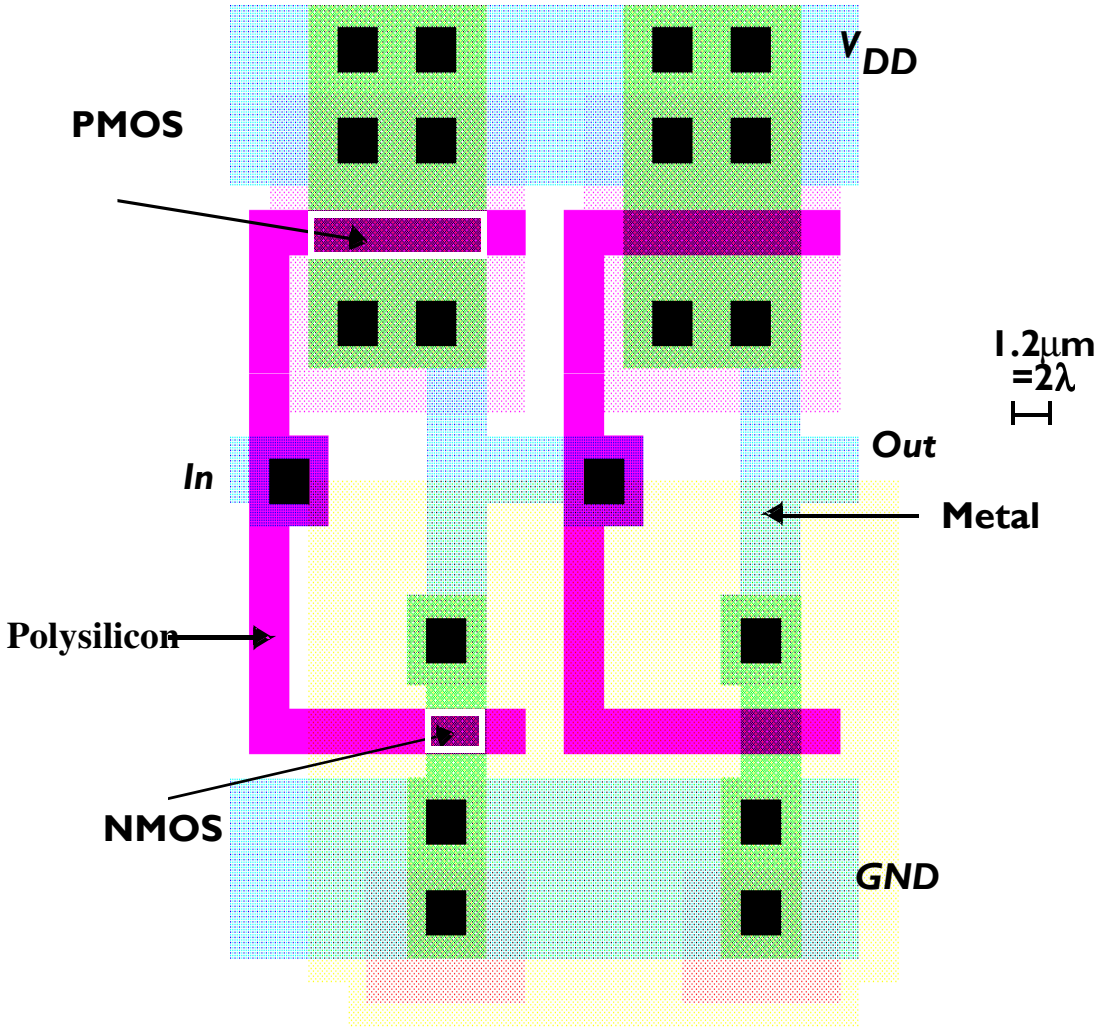


Stick Diagram



Layout

CMOS Inverter Layout



4-Input NAND Gate