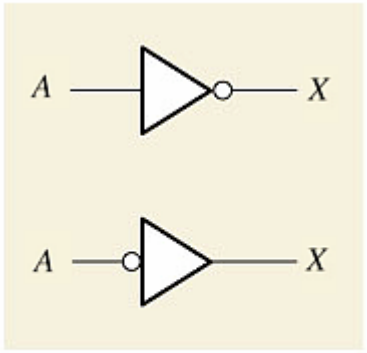
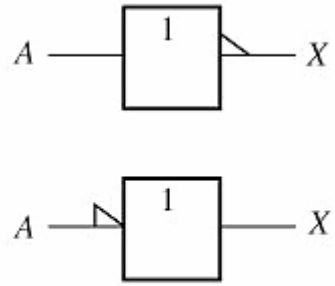
Logic Gates

- Inverter
- AND Gate
- OR Gate
- Exclusive-OR Gate
- NAND Gate
- NOR Gate
- Exclusive-NOR Gate
- Transmission Gate
- IC

The Inverter



Distinctive shape symbols



Rectangular outline symbols

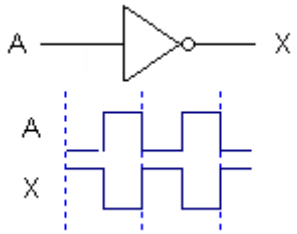
A	X
0	1
1	0

Truth table

$X = \overline{A}$

Boolean expression

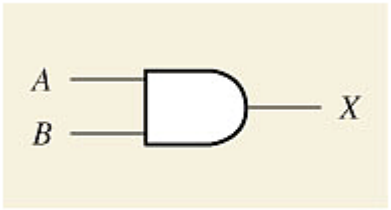
0 = LOW
1 = HIGH



Pulsed waveforms

The output of an inverter is always the complement (opposite) of the input.

The AND Gate



Distinctive shape symbol

Rectangular outline symbol

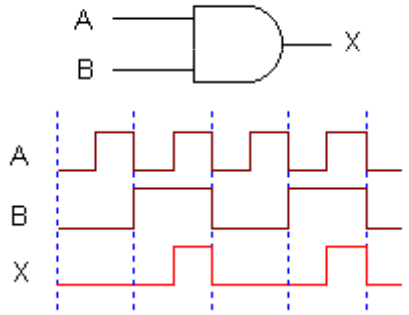
A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

Truth table

0 = LOW
1 = HIGH

$X = AB$

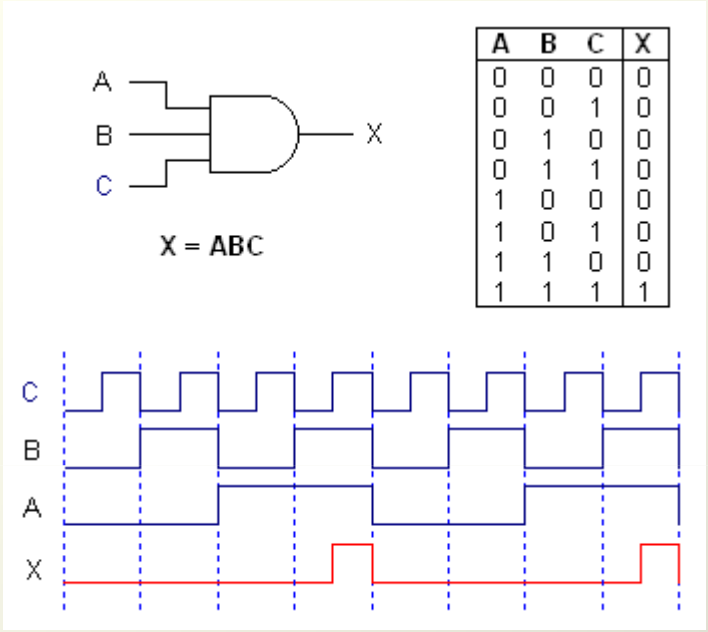
Boolean expression



Pulsed waveforms

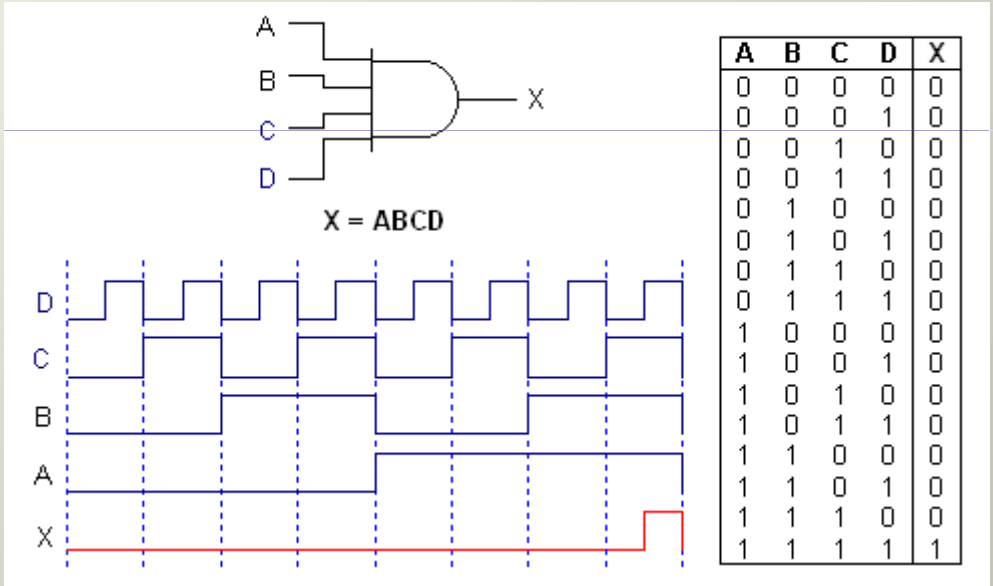
The output of an AND gate is HIGH only when all inputs are HIGH.

The AND Gate



A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

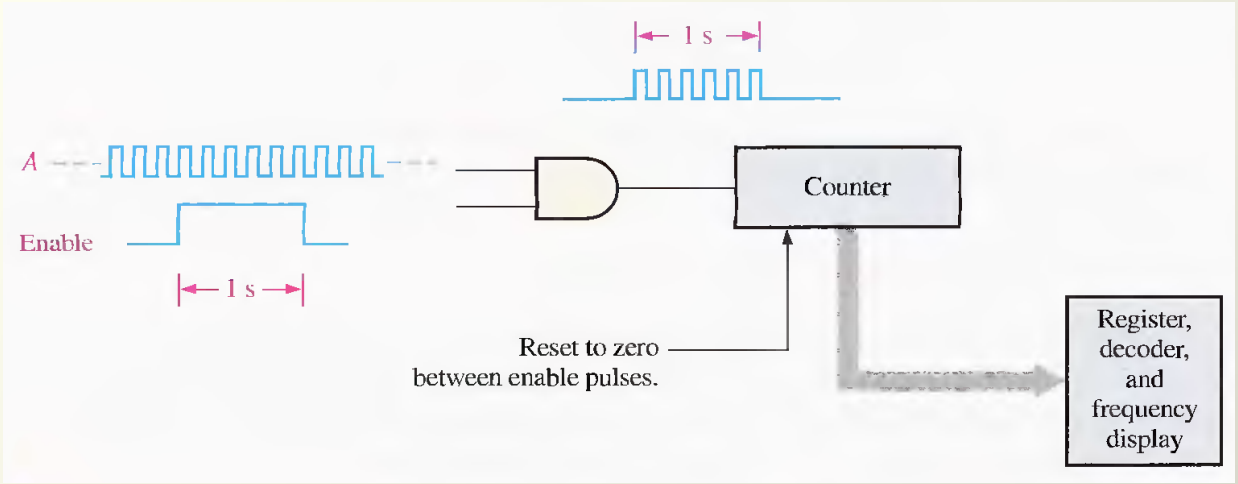
3-Input AND Gate



A	B	C	D	X
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

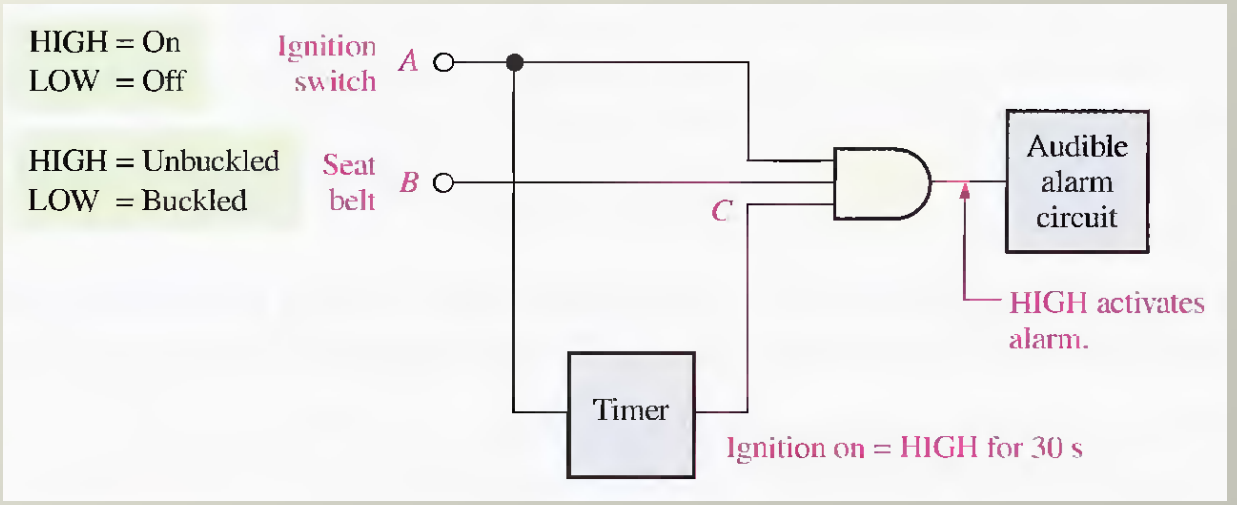
4-Input AND Gate

AND Gate Applications

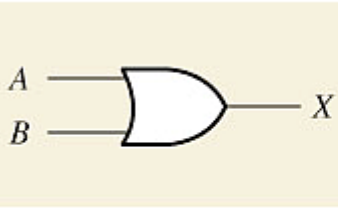


Frequency Counter

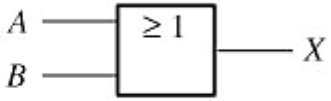
Seat Belt Alarm



The OR Gate



Distinctive shape symbol



Rectangular outline symbol

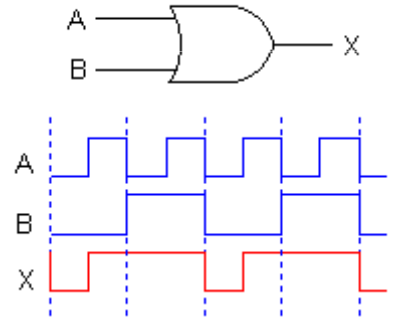
A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

Truth table

0 = LOW
1 = HIGH

$X = A + B$

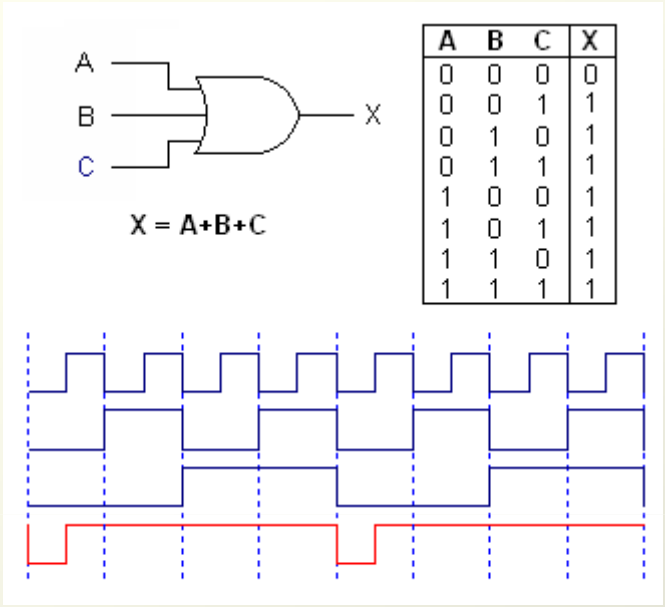
Boolean expression



Pulsed waveforms

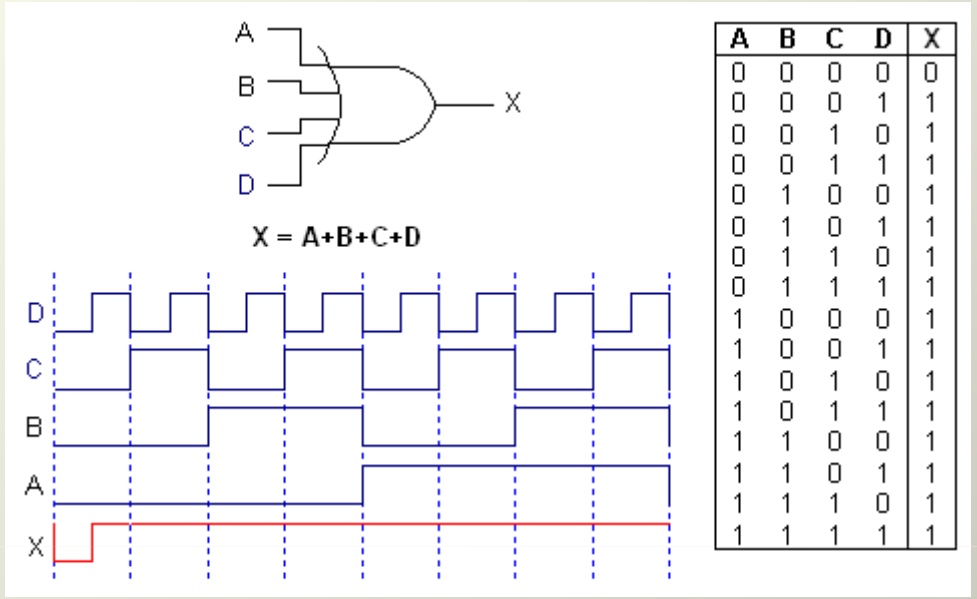
The output of an OR gate is HIGH whenever one or more inputs are HIGH

The OR Gate



A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

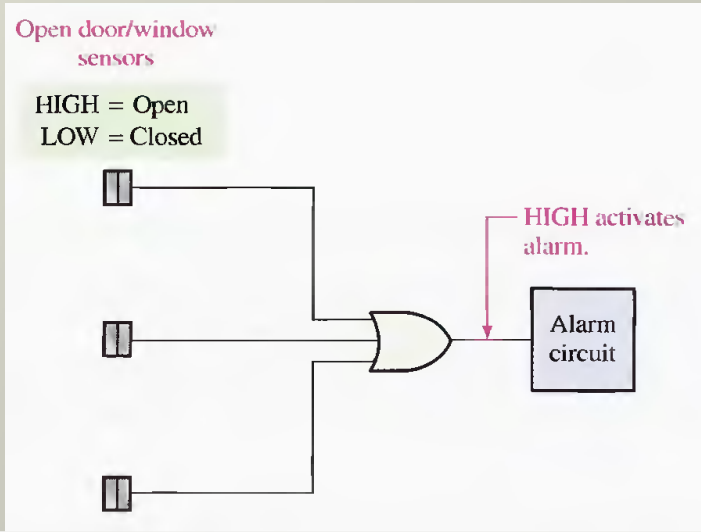
3-Input OR Gate



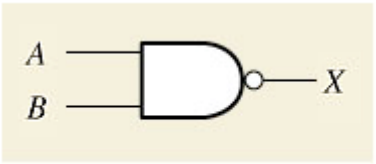
A	B	C	D	X
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

4-Input OR Gate

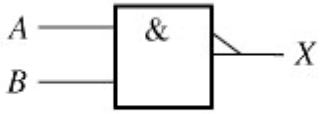
Intrusion Detection



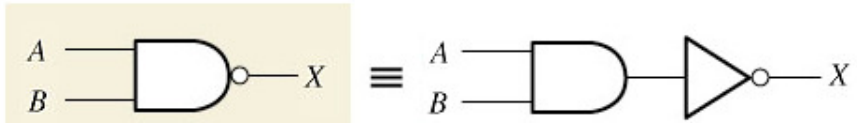
The NAND Gate



Distinctive shape symbol



Rectangular outline symbol



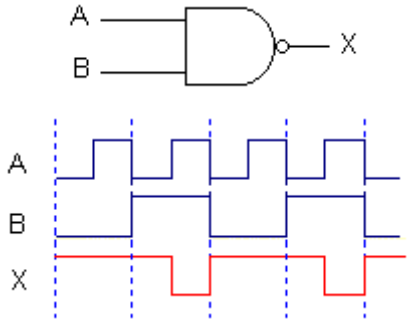
A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

Truth table

0 = LOW
1 = HIGH

$X = \overline{AB}$

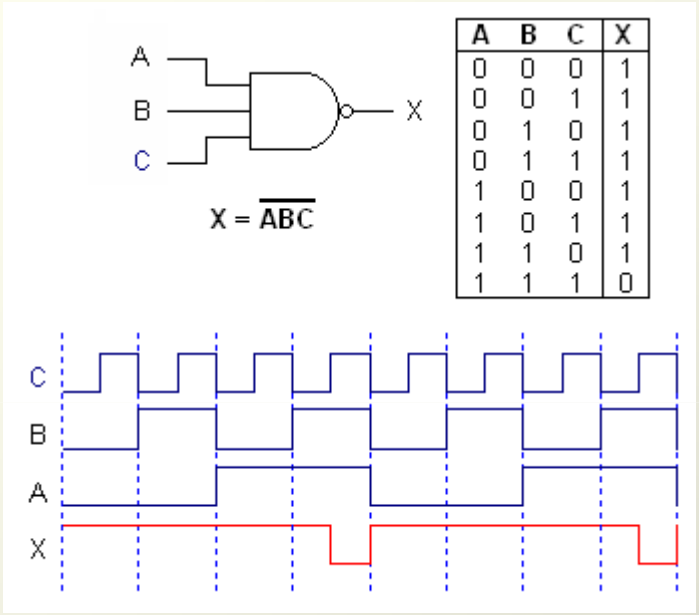
Boolean expression



Pulsed waveforms

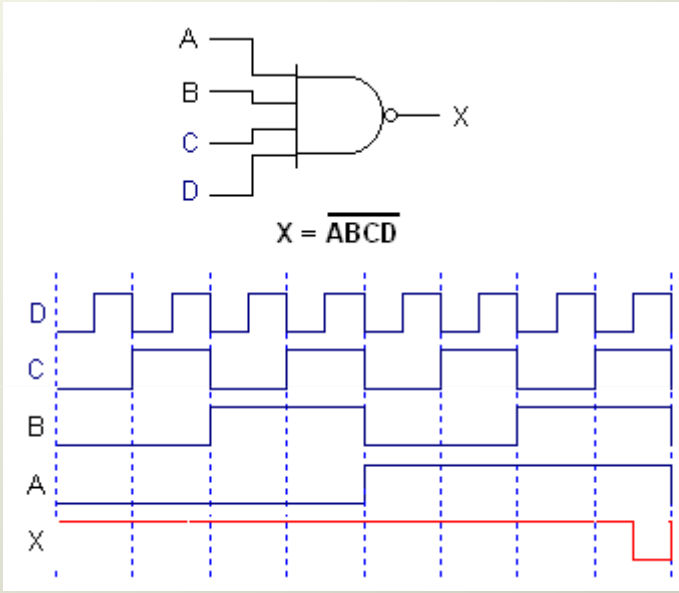
The output of a NAND gate is HIGH whenever one or more inputs are LOW.

The NAND Gate



A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

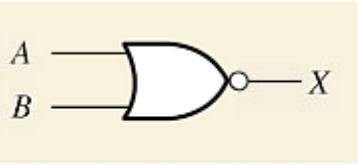
3-Input NAND Gate



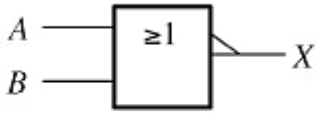
A	B	C	D	X
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

4-Input NAND Gate

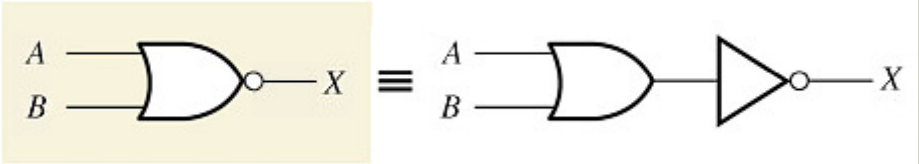
The NOR Gate



Distinctive shape symbol



Rectangular outline symbol



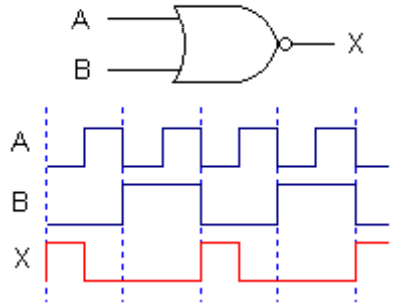
A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

Truth table

0 = LOW
1 = HIGH

$X = \overline{A + B}$

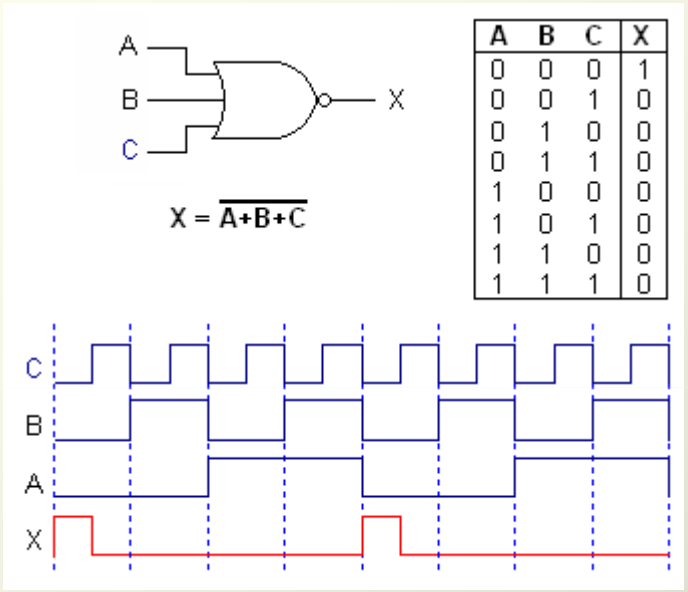
Boolean expression



Pulsed waveforms

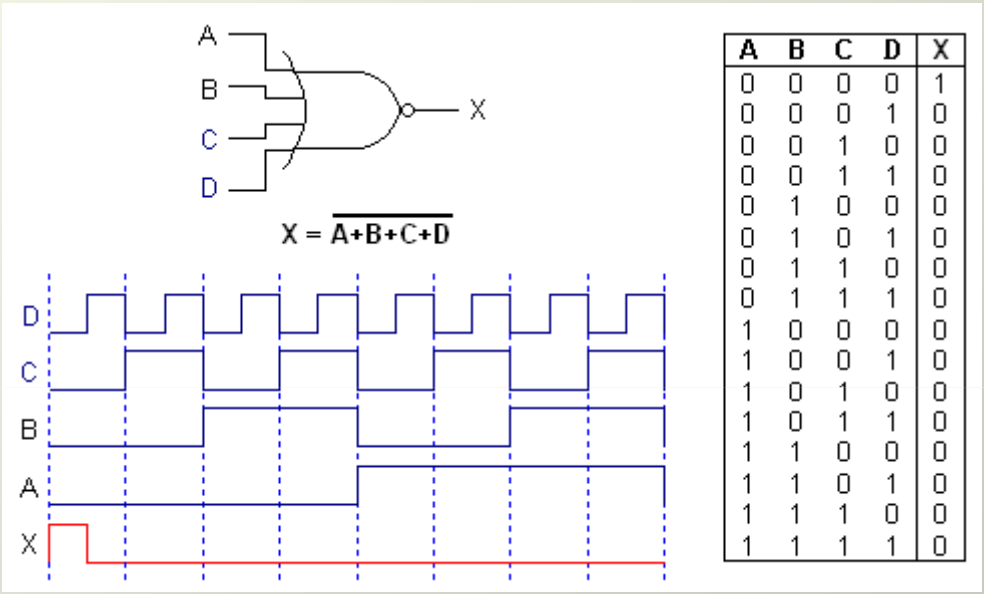
The output of a NOR gate is LOW whenever one or more inputs are HIGH.

The NOR Gate



A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

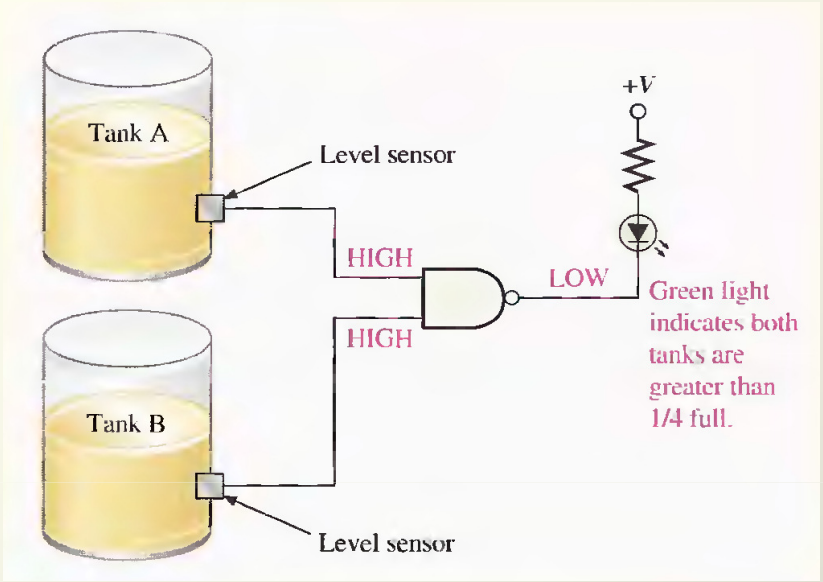
3-Input NOR Gate

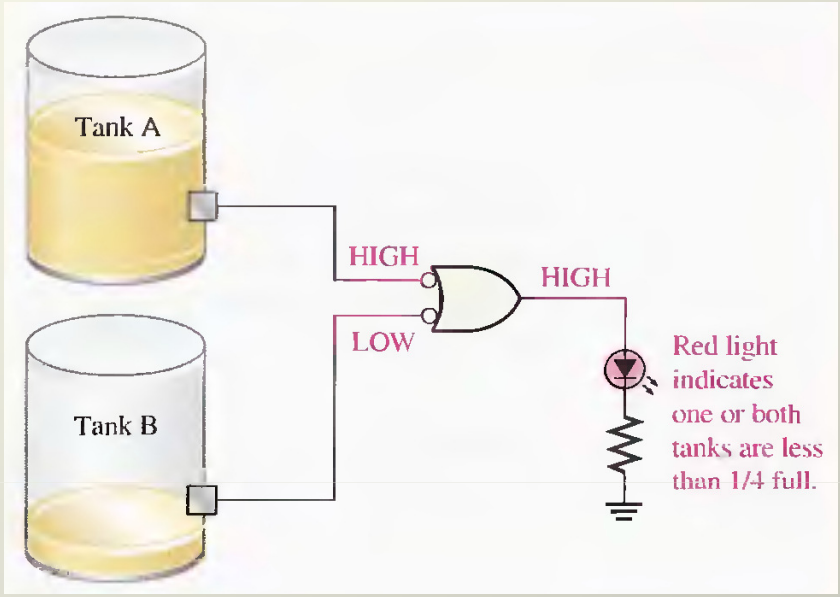


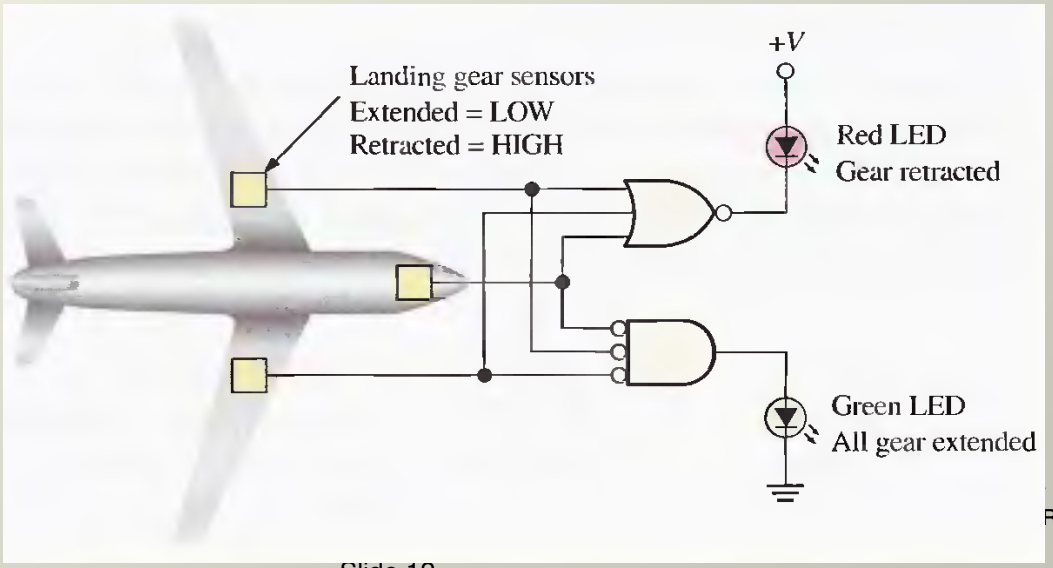
A	B	C	D	X
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

4-Input NOR Gate

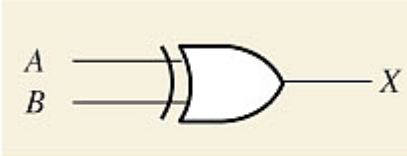
NAND & NOR Gates Applications



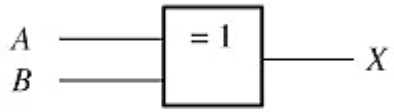




Exclusive-OR Gate



Distinctive shape symbol



Rectangular outline symbol

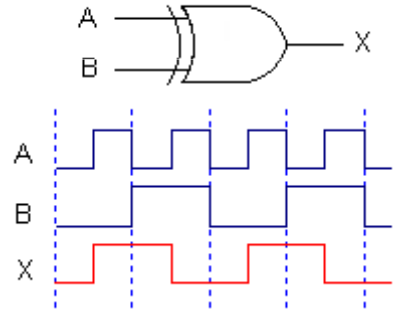
A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

Truth table

0 = LOW
1 = HIGH

$X = A \oplus B$

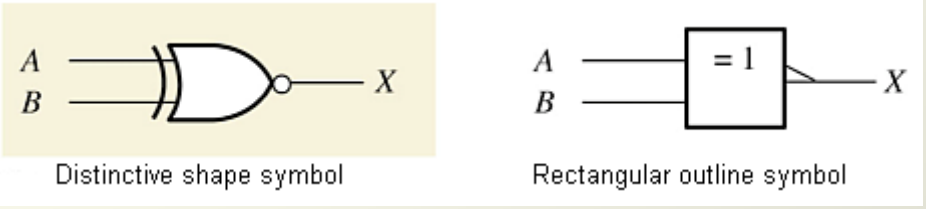
Boolean expression



Pulsed waveforms

The output of an XOR gate is HIGH whenever the two inputs are different.

Exclusive-NOR Gate



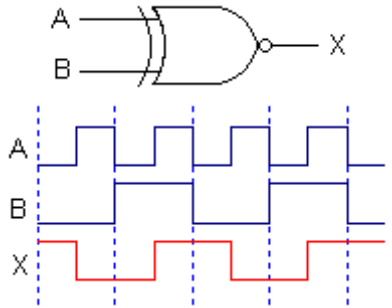
A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

Truth table

0 = LOW
1 = HIGH

$X = \overline{A \oplus B}$

Boolean expression

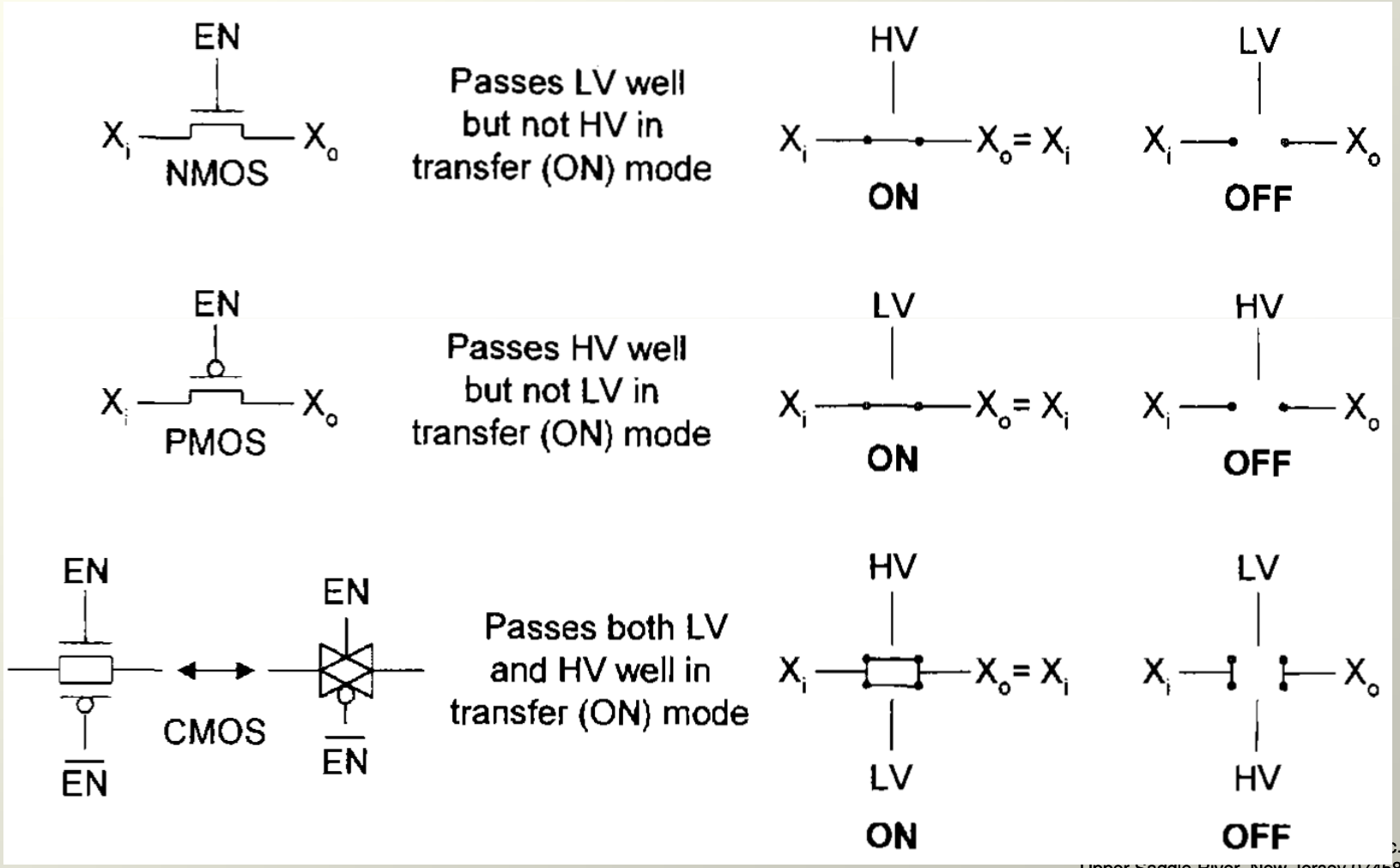


Pulsed waveforms

The output of an XNOR gate is HIGH whenever the two inputs are identical.

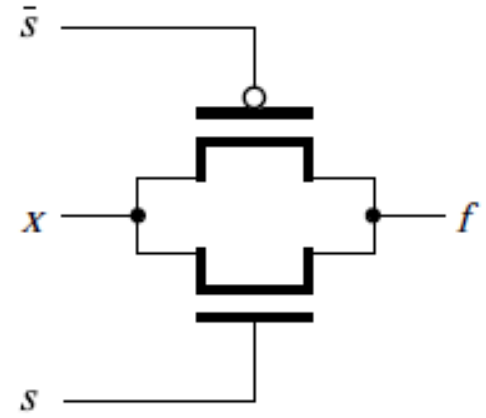
Transmission Gates

- NMOS passes 0 well, but not 1; PMOS does the opposite.
- *Transmission gates* pass both 0 and 1 well



*Tinder's engineering digital design

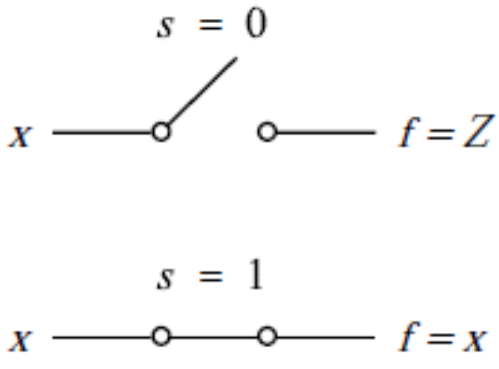
Transmission Gates



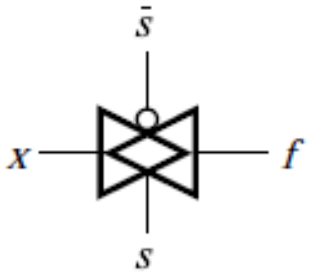
(a) Circuit

s	f
0	Z
1	x

(b) Truth table



(c) Equivalent circuit

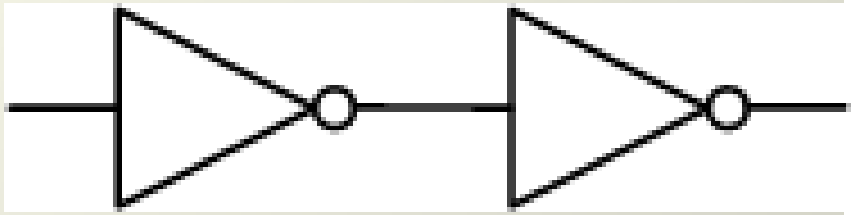


(d) Graphical symbol

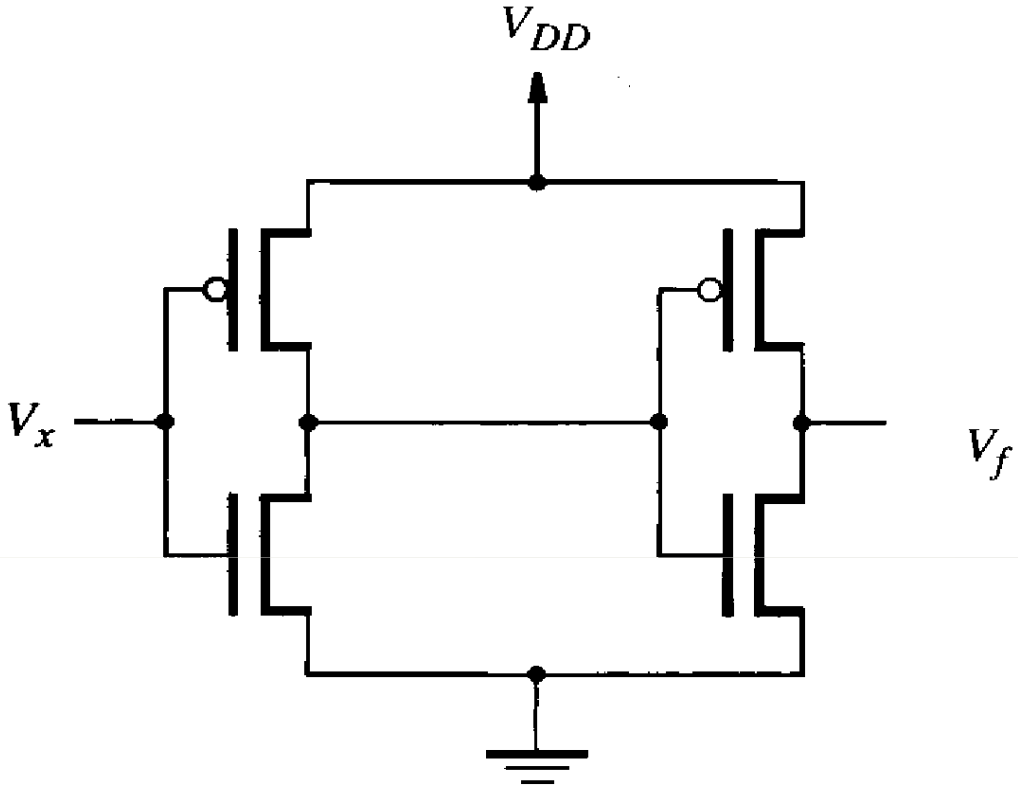
*Brown's fundamentals of digital logic

Noninverting Buffer

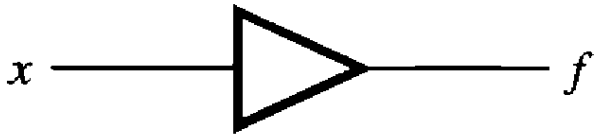
The buffer is a single-input device which has a gain of 1, mirroring the input at the output. It has value for impedance matching (high-to-low) and for isolation of the input and output. Typically, it is used to deliver higher power to drive a large capacitive load.



*Brown's fundamentals of digital logic

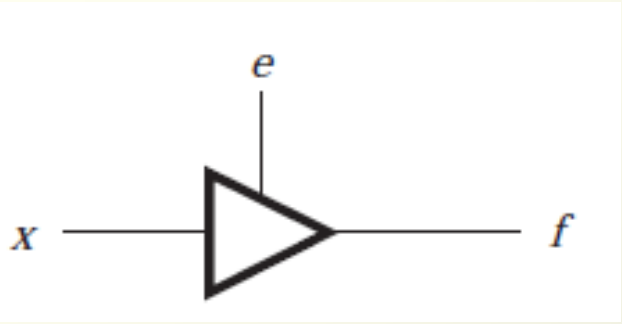


(a) Implementation of a buffer

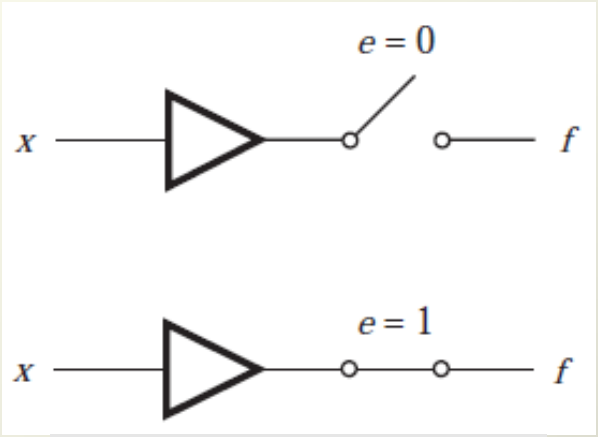


(b) Graphical symbol

Tri-state Buffer



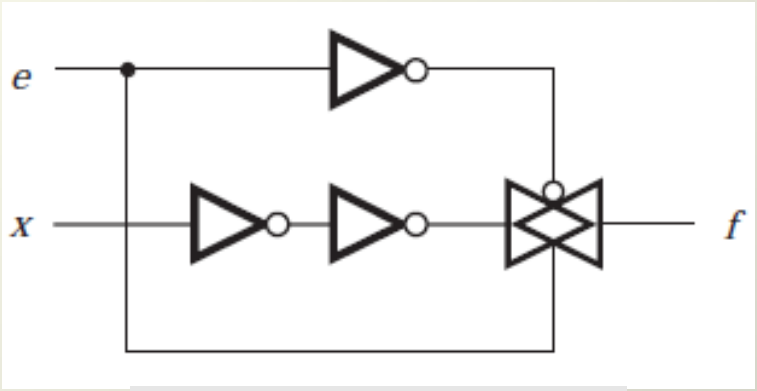
Symbol



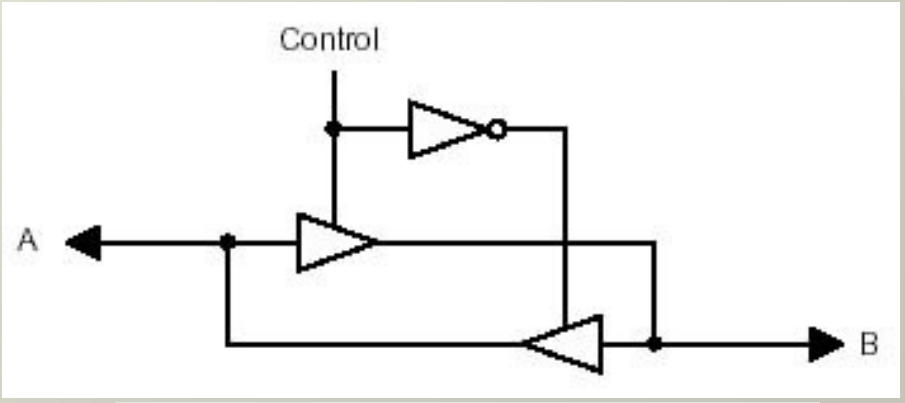
Equivalent Circuit

e	x	f
0	0	Z
0	1	Z
1	0	0
1	1	1

Truth Table



Implementation



Application Example

*Brown's fundamentals of digital logic

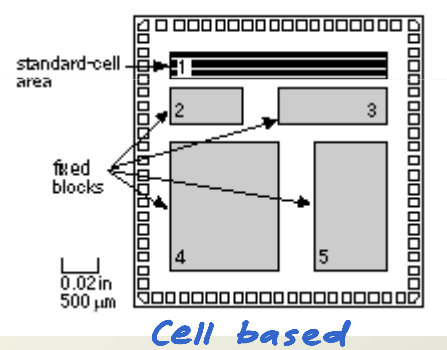
Types of ICs

Design Style

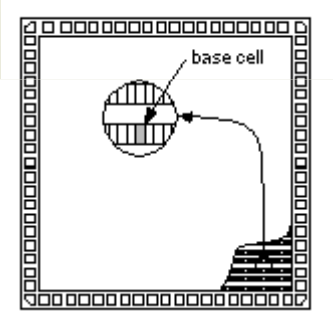
- ASSP
- ASIC

Use

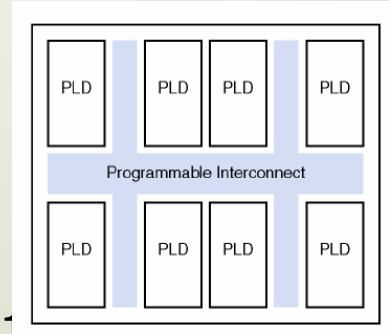
- Full-custom
- Semi-custom
  - Cell Based
  - Gate Arrays
- Programmable
  - CPLD and FPGA



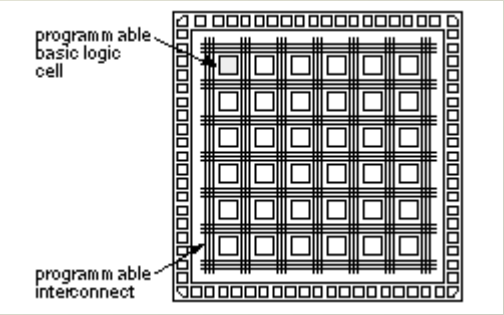
Cell based



Gate Array



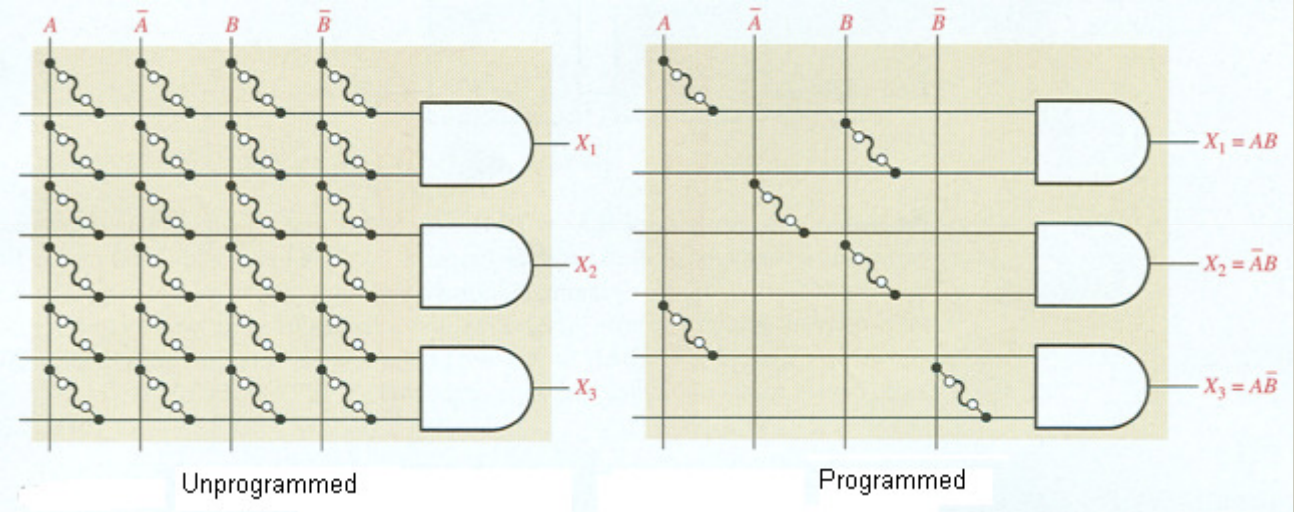
CPLD



FPGA

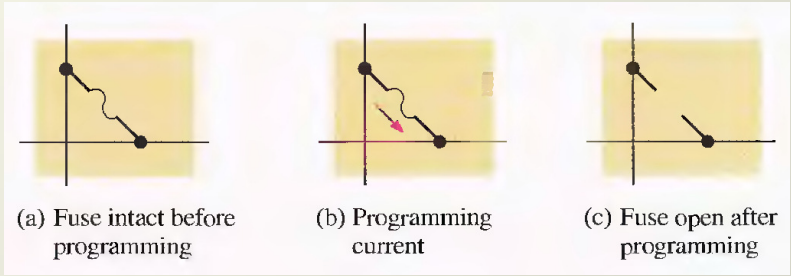
Programmable Logic Device (PLD)

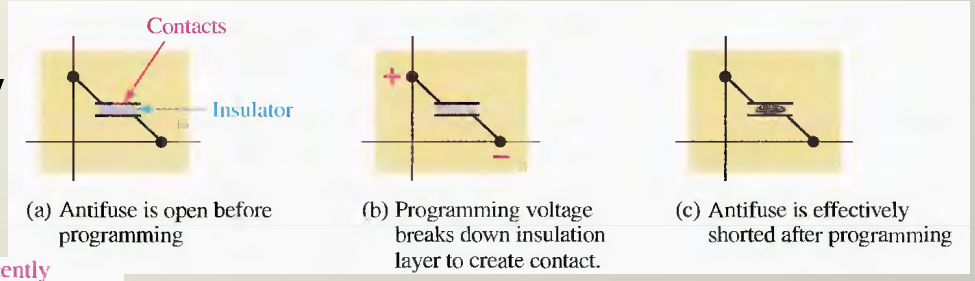
- Programmable AND array

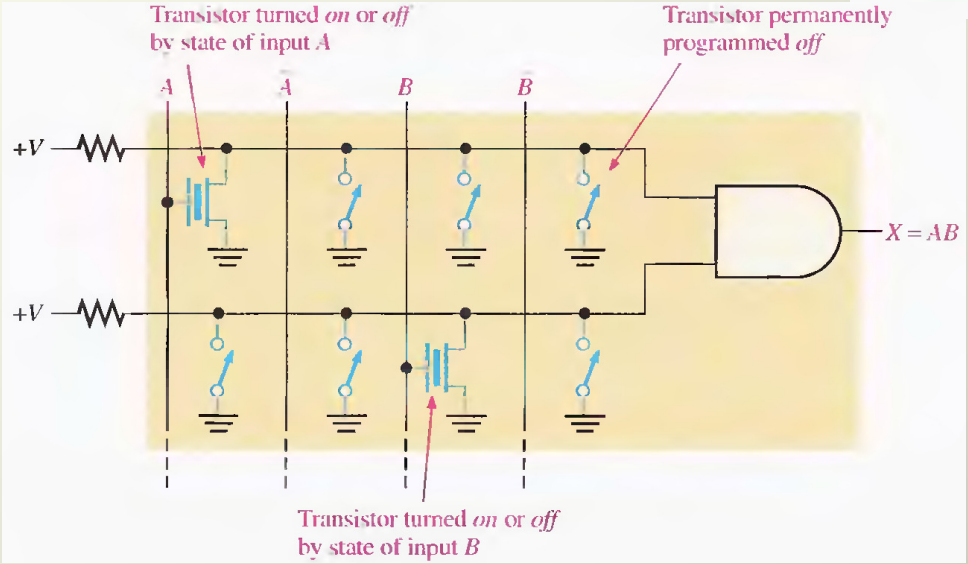


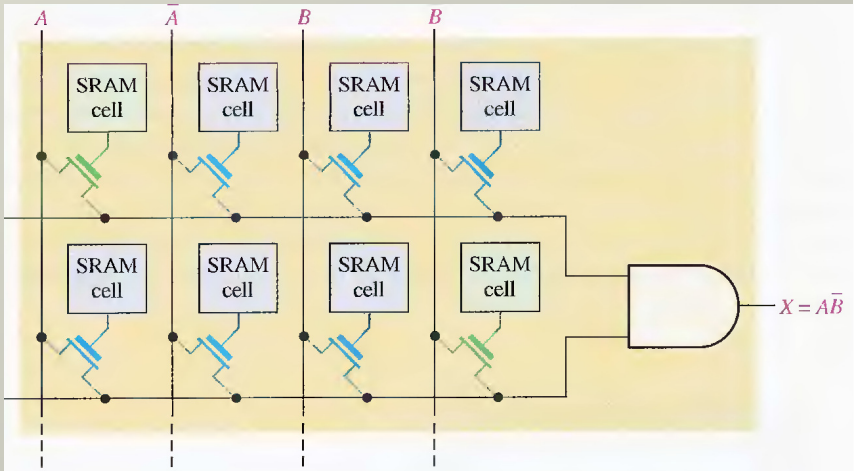
Programmable link technology

- Fuse technology
- Anti-fuse technology
- EPROM technology
- EEPROM technology
- SRAM technology



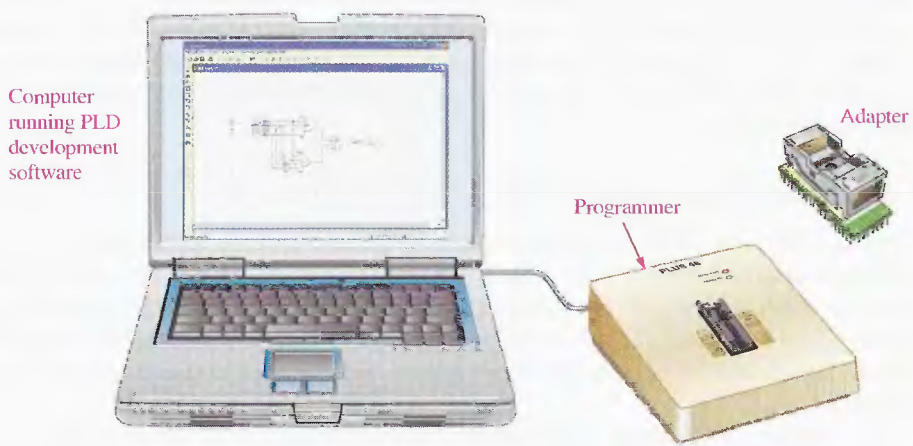


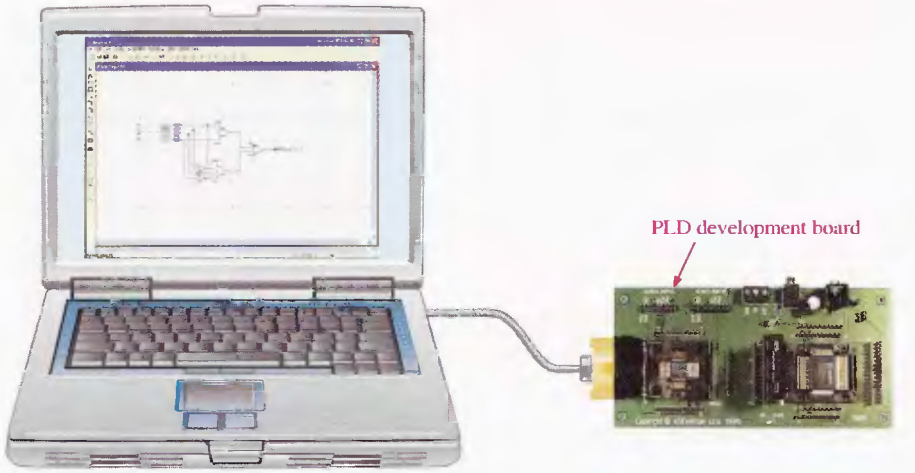




Device programming

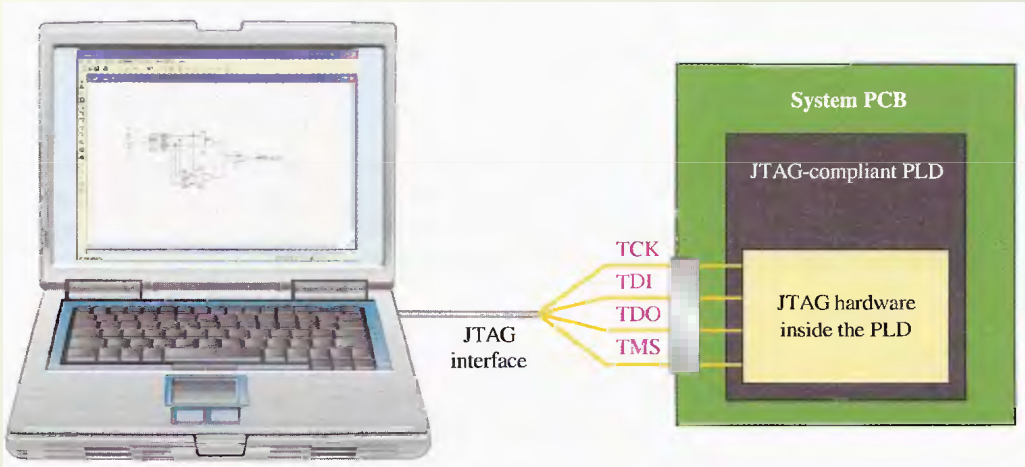
- Design entry
  - Text entry
  - Graphic (schematic) entry

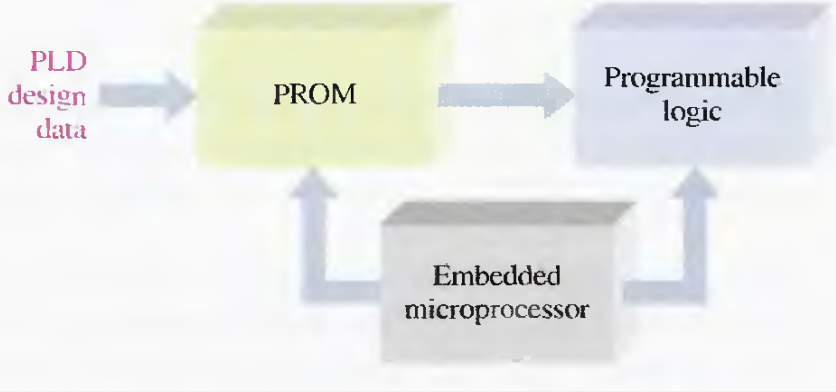




Programmable Logic

- In-system programming (ISP)
  - Joint Test Action Group (JTAG)
  - Embedded processor

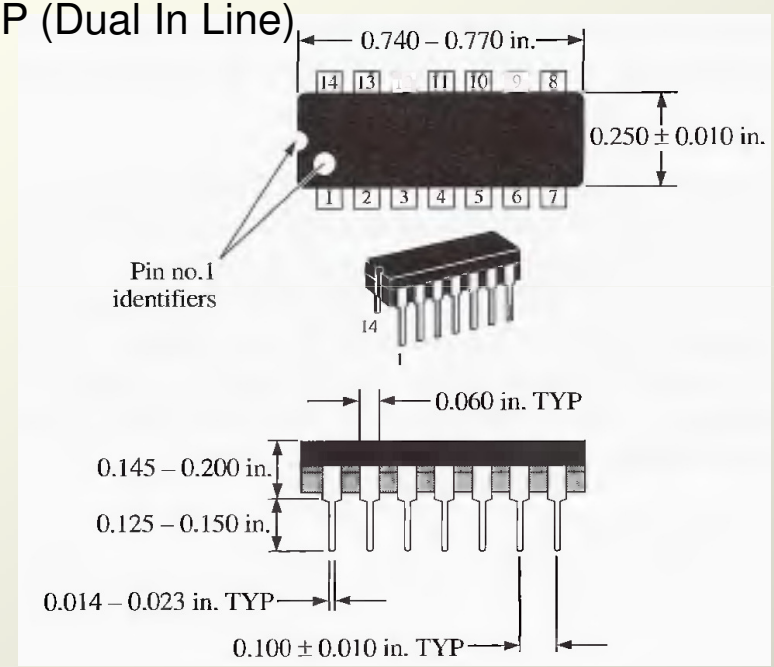


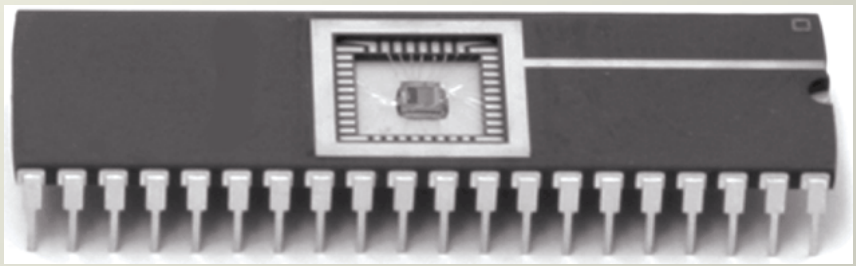


Fixed-Function Logic

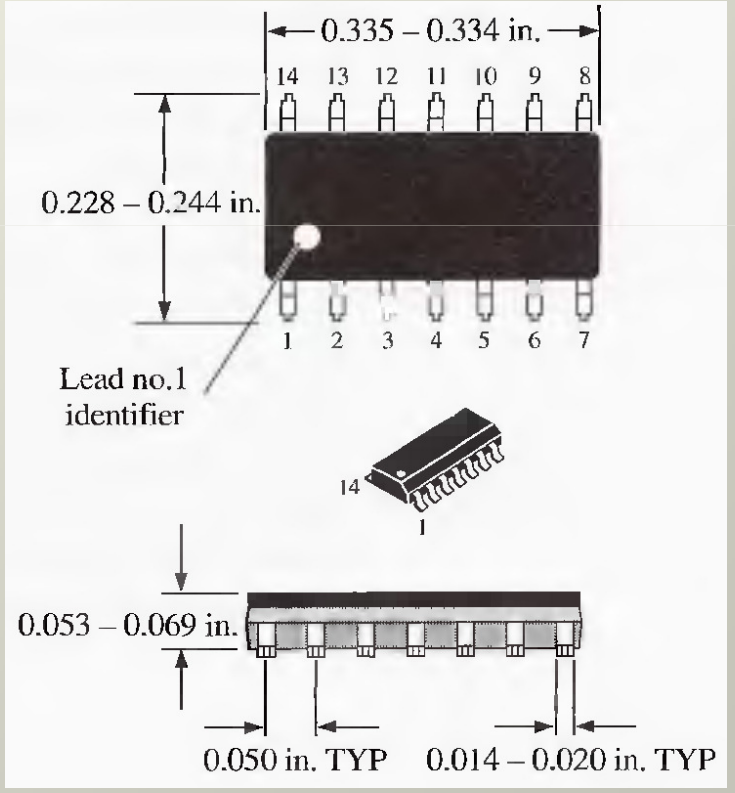
- CMOS
- TTL (Transistor-Transistor Logic)

DIP (Dual In Line)

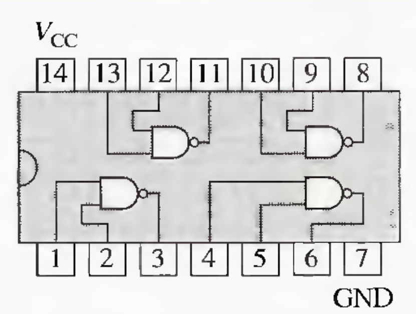


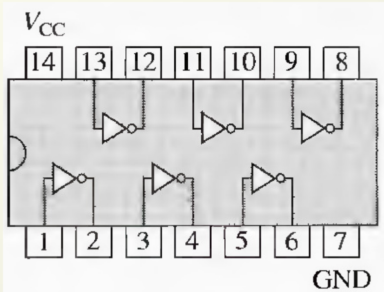


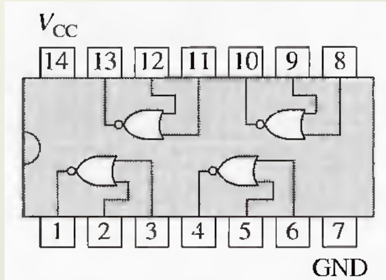
SOIC (Small Outline IC

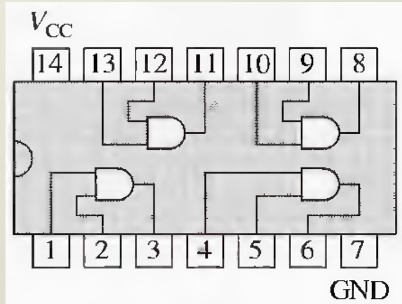


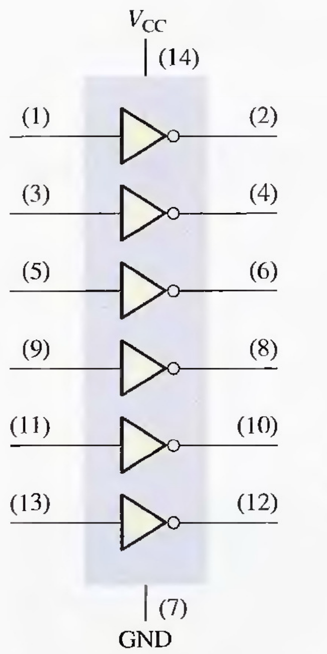
IC Gates



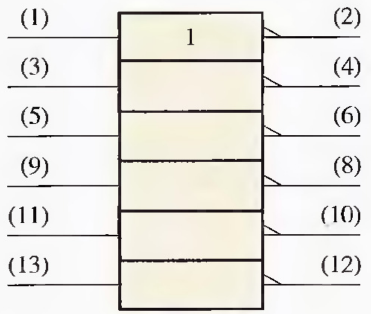




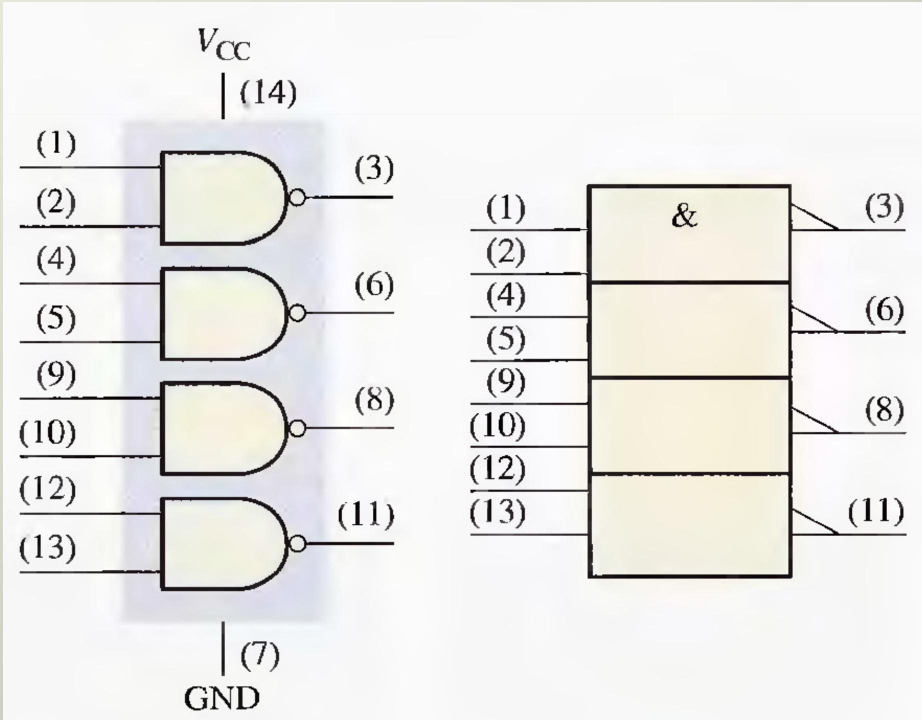




Distinctive shape logic diagram



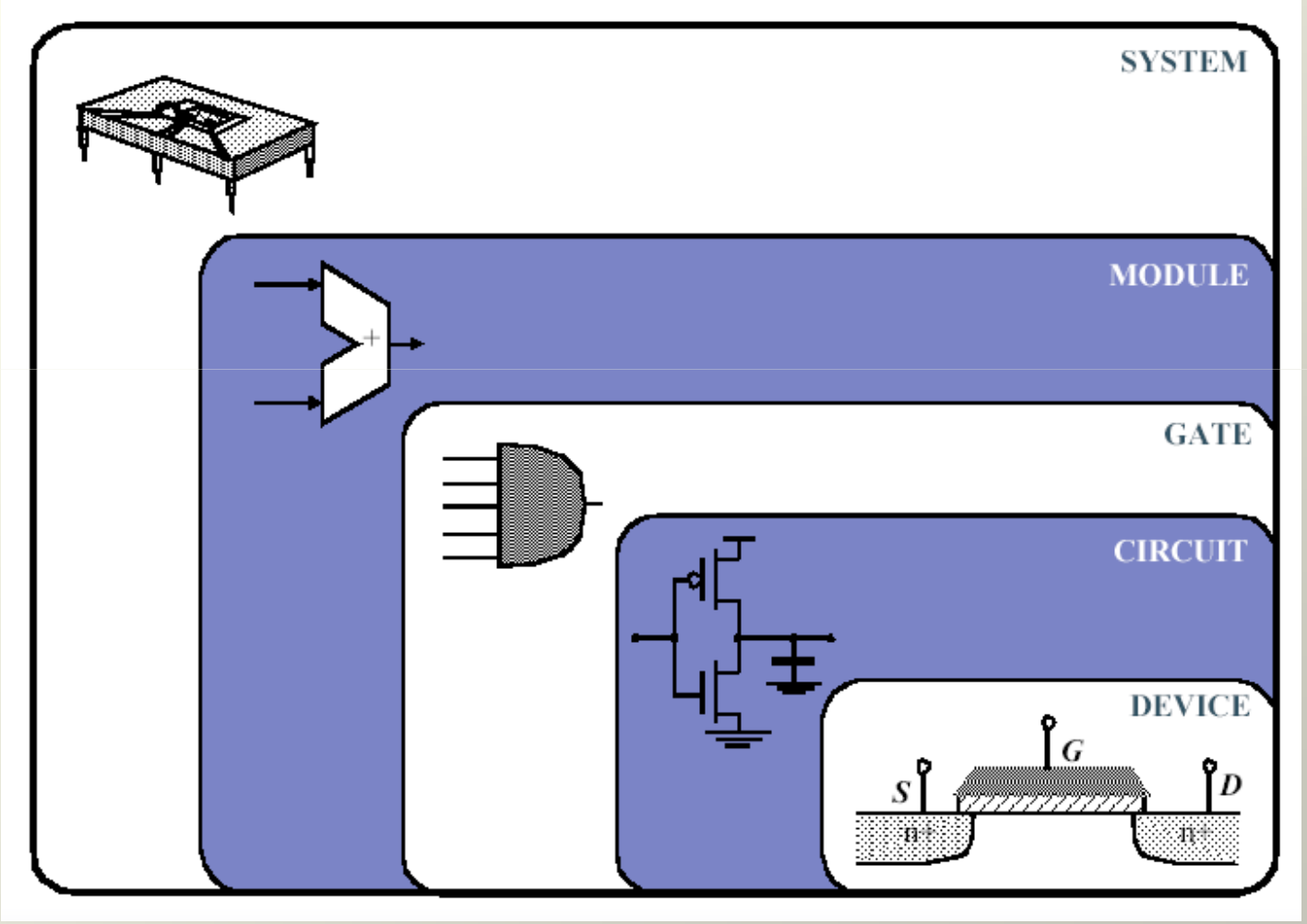
Rectangular outline logic symbol with polarity indicators. The inverter qualifying symbol (1) appears in the top block and applies to all blocks below.



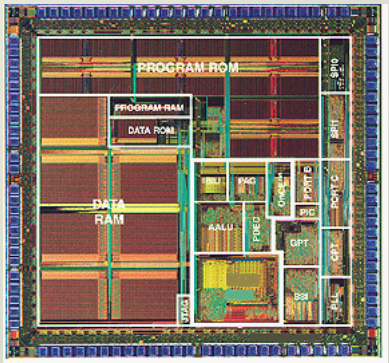
Chip Integration Level

- **SSI** = small-scale integration
  (up to 10 gates)
- **MSI** = medium-scale integration
  (up to 1000 gates)
- **LSI** = large-scale integration
  (up to 10000 gates)
- **VLSI** = very large-scale integration
  (over 10000 gates)

Design Abstraction Levels



Design Abstraction Levels



RTL SW

System Level

RTL

Register Transfer Level (Hardware Description Language (HDL))

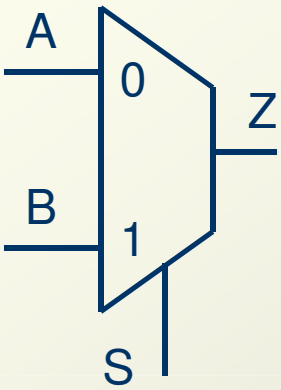
Gate Level

Transistor Level

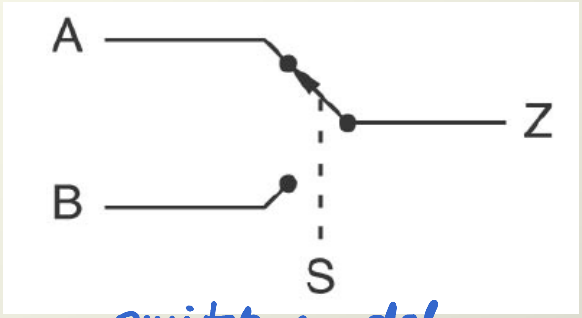
Abstraction

1970 1980 1990 2000+

A mux at different levels of abstraction



symbol for multiplexer function



switch model for multiplexer

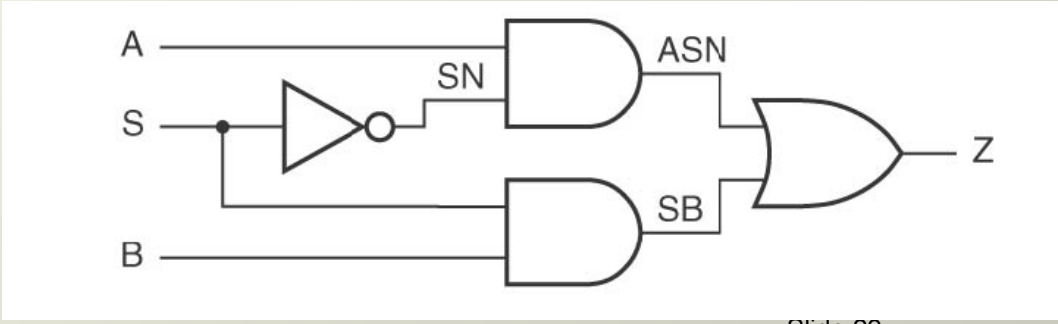
multiplexer function logic equation

$$Z = A \cdot S' + B \cdot S$$

multiplexer truth table

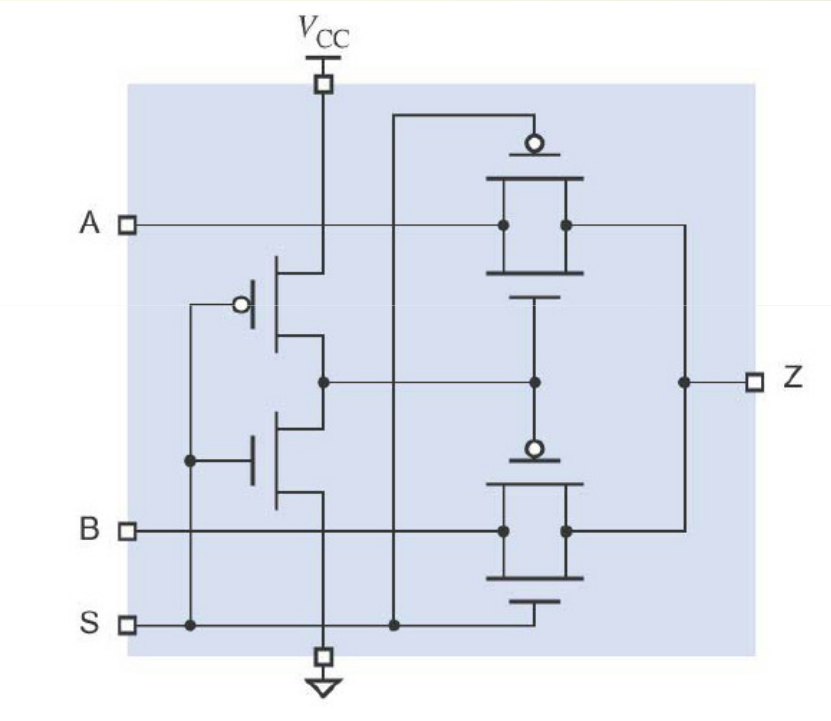
S	A	B	Z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

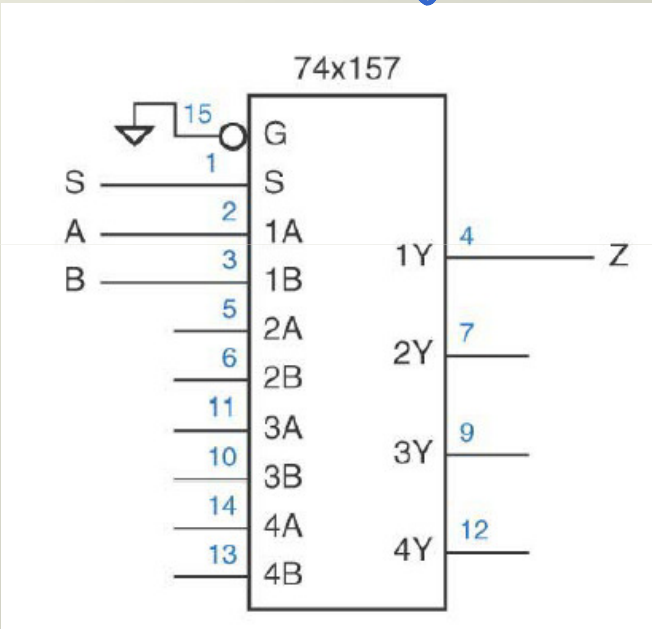
gate-level logic diagram for mux



A mux at different levels of abstraction

multiplexer using an MSI building block





multiplexer desing using MOS transistors